HYM564224A X-Series

Buffered 2Mx64 bit CMOS DRAM MODULE
based on 1Mx16 DRAM, EDO, 1K-Refresh

GENERAL DESCRIPTION

The HYM564224A X-Series is a 2Mx64-bit Extended Data Out mode CMOS DRAM module consisting of eight HY5118164B in 42 pin SOJ and two 16-bit BiCMOS line driver in TSSOP on a 168 pin glass-epoxy printed circuit board. 0.1µF and 0.01µF decoupling capacitors are mounted for each DRAM.
The HYM564224AXG is Gold plated socket type Dual In-line Memory Module suitable for easy interchange and addition of 16M byte memory.

FEATURES

- 168-Pin Buffered DIMM
- Extended Data Out Operation
- /CAS-before-/RAS, /RAS-only,
  Hidden and Self refresh capability
- 1024 refresh cycles / 256ms (SL-part)
  1024 refresh cycles / 16ms
- Fast access time and cycle time

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- TTL compatible inputs and outputs
- JEDEC standard pinout
- Buffered inputs (except /RAS and DQ)
- 4 Byte interleave enabled,
  Dual address inputs (A0,B0)
- Single power supply of 5V±10%
- Low power dissipation

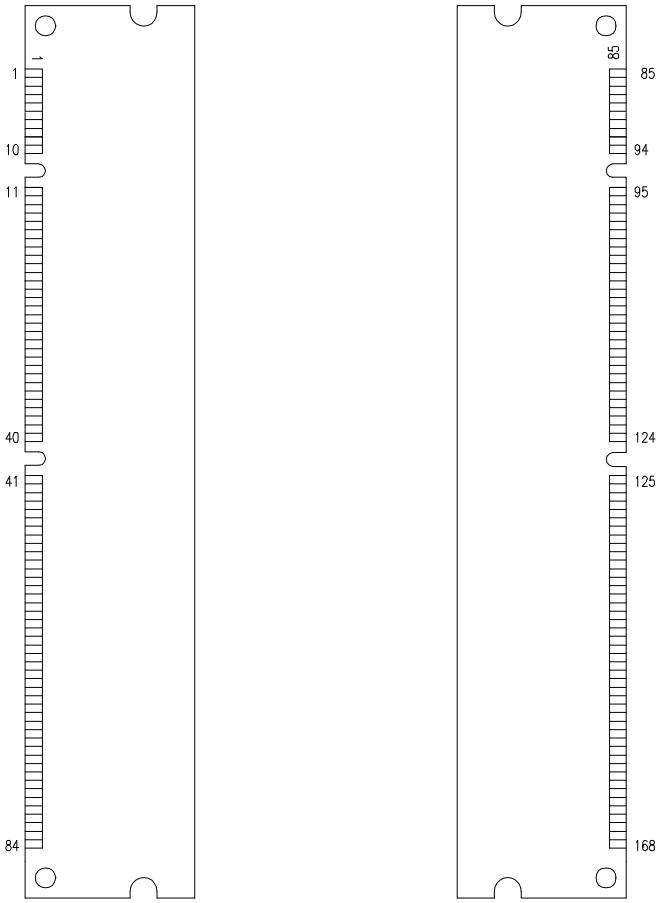
  Max. self-refresh : 37.4mW (SL-part)
  Max. battery back-up : 41.8mW (SL-part)
  Max. CMOS standby : 35.2mW (SL-part)
  66mW
  Max. TTL standby : 110mW
  Max. operating

Speed	Power
60	3.92W
70	3.70W
80	3.48W

ORDERING INFORMATION

PART NUMBER	SPEED	FEATURES	PACKAGE	PLATING
HYM564224AXG	60/70/80	EDO, 1K, 5V	DIMM	Gold
HYM564224ATXG	60/70/80	EDO, 1K, 5V	DIMM	Gold

PIN CONNECTION



PIN DISCRIPTION

/RAS0~/RAS3	Row Address Strobe
/CAS0~/CAS7	Column Address Strobe
/WE0, /WE2	Write Enable
/OE0, /OE2	Output Enable
A0-A9, B0	Address Input
DQ0-DQ63	Data Input / Output
PD1~PD8	Presence Detect
/PDE	Presence Detect Enable
ID0, ID1	ID Bit
VCC	Power (+5V)
VSS	Ground

PIN ASSIGNMENTS

#	NAME	#	NAME	#	NAME	#	NAME
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	/OE2	86	DQ32	128	NC
3	DQ1	45	/RAS2	87	DQ33	129	/RAS3
4	DQ2	46	/CAS4	88	DQ34	130	/CAS5
5	DQ3	47	/CAS6	89	DQ35	131	/CAS7
6	VCC	48	/WE2	90	VCC	132	/PDE
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	DQ16	94	DQ39	136	DQ48
11	NC	53	DQ17	95	NC	137	DQ49
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ8	55	DQ18	97	DQ40	139	DQ50
14	DQ9	56	DQ19	98	DQ41	140	DQ51
15	DQ10	57	DQ20	99	DQ42	141	DQ52
16	DQ11	58	DQ21	100	DQ43	142	DQ53
17	DQ12	59	VCC	101	DQ44	143	VCC
18	VCC	60	DQ22	102	VCC	144	DQ54
19	DQ13	61	NC	103	DQ45	145	NC
20	DQ14	62	NC	104	DQ46	146	NC
21	DQ15	63	NC	105	DQ47	147	NC
22	NC	64	NC	106	NC	148	NC
23	VSS	65	DQ23	107	VSS	149	DQ55
24	NC	66	NC	108	NC	150	NC
25	NC	67	DQ24	109	NC	151	DQ56
26	VCC	68	VSS	110	VCC	152	VSS
27	/WE0	69	DQ25	111	NC	153	DQ57
28	/CAS0	70	DQ26	112	/CAS1	154	DQ58
29	/CAS2	71	DQ27	113	/CAS3	155	DQ59
30	/RAS0	72	DQ28	114	/RAS1	156	DQ60
31	/OE0	73	VCC	115	NC	157	VCC
32	VSS	74	DQ29	116	VSS	158	DQ61
33	A0	75	DQ30	117	A1	159	DQ62
34	A2	76	DQ31	118	A3	160	DQ63
35	A4	77	NC	119	A5	161	NC
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	VCC	82	PD7	124	VCC	166	PD8
41	NC	83	ID0(VSS)	125	NC	167	ID1
42	NC	84	VCC	126	B0	168	VCC

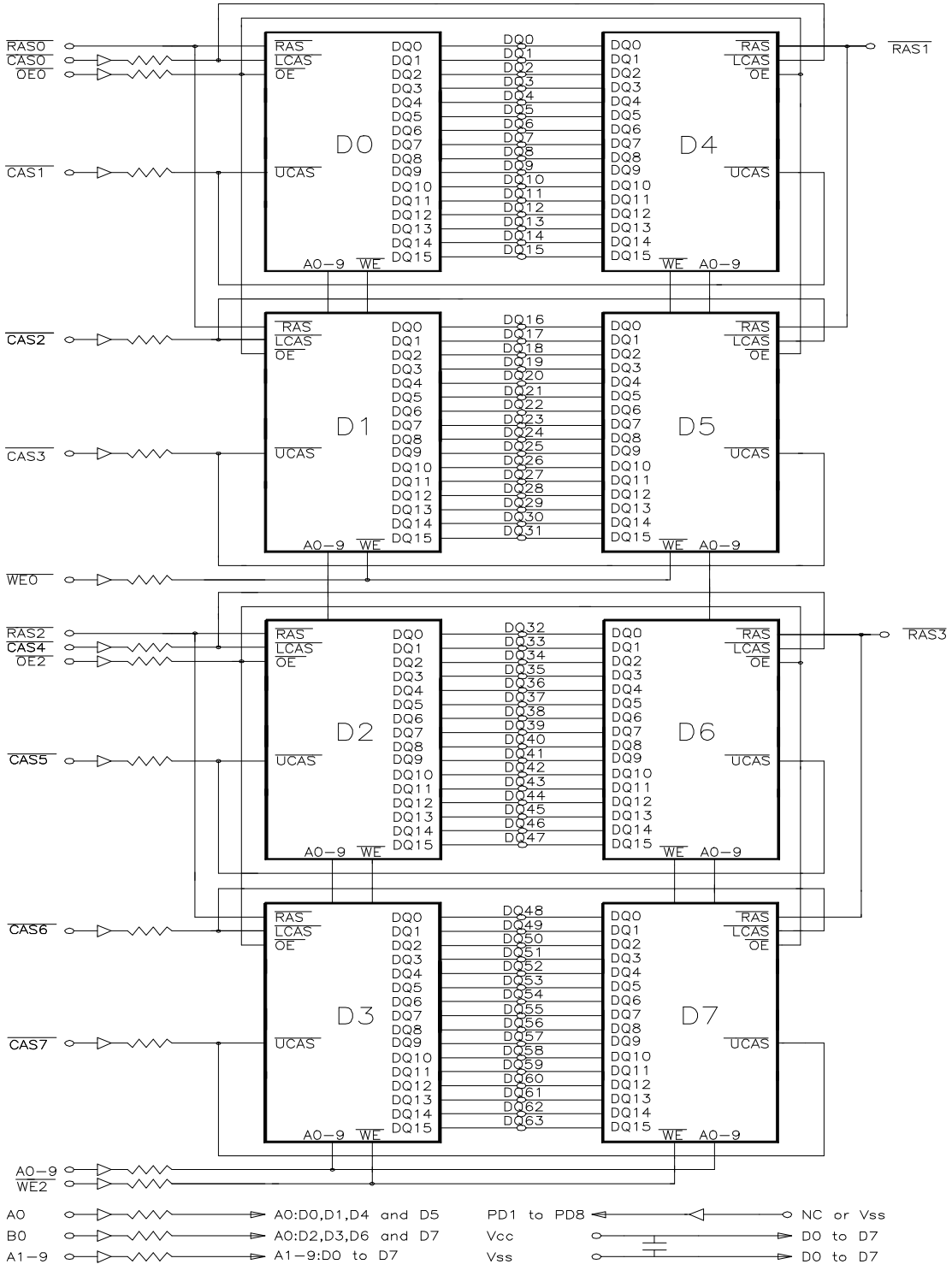
PRESENCE DETECT PINS

PIN	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	ID0	ID1
60	VSS	VSS	VSS	NC	NC	NC	NC	NC	VSS	NC or VSS
70	VSS	VSS	VSS	NC	NC	VSS	NC	NC	VSS	NC or VSS
80	VSS	VSS	VSS	NC	NC	NC	VSS	NC	VSS	NC or VSS

NOTE :

1. PDs are either open NC or Driven to VSS via on-board buffer circuits.
2. IDs are connected directly to NC or VSS without a buffer.
3. ID1 will be either open NC for Self-Refresh or driven to VSS for standard.

BLOCK DIAGRAM



NOTE : All resistors are 25 Ohm ± 5%

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin relative to VSS	-0.5 to 4.6	V
VCC	Voltage on VCC relative to VSS	-0.5 to 4.6	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	9.7	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(T_A=0°C to 70°C, VCC=5V ± 10% and VSS=0V, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current 1K Ref	UNIT
ICC1	Operating Current	/RAS and /CAS cycling tRC=tRC (min.)	60 70 80	712 672 632	mA
ICC2	TTL Standby Current	/RAS = /CAS ≥ VIH other inputs ≥ VSS		20	mA
ICC3	/RAS-only Refresh Current	/CAS = VIH, /RAS cycling tRC = tRC (min.)	60 70 80	712 672 632	mA
ICC4	EDO Mode Current	/RAS = VIL, /CAS, Address cycling tHPC = tHPC (min.)	60 70 80	632 552 472	mA
ICC5	CMOS Standby Current	/RAS = /CAS ≥ VCC-0.2V	 SL-part	12 6.4	mA mA
ICC6	/CAS-before-/RAS Refresh Current	/RAS and /CAS cycling tRC=tRC (min.)	60 70 80	712 672 632	mA
ICC7	Battery Back-up Current (SL-part)	tRC=250µs /CAS = CBR cycling or 0.2V /OE & /WE=VCC - 0.2V Address =VCC-0.2V or 0.2V DQ0-DQ3 =VCC-0.2V, 0.2V or open	tRAS ≤ 300ns	6.8	mA
			tRAS ≤ 1µs	7.6	mA
ICC8	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as ICC7		6.8	mA

Symbol	Parameter	Test condition		Min.	Max.	UNIT
ILI	Input Leakage current (Any Input)	VSS ≤ VIN ≤ VCC + 1.0 All other pins not under test=VSS	All but /RAS /RAS	-10 -20	10 20	µA
ILO	Output Leakage current (Any Input)	VSS ≤ VOUT ≤ VCC /RAS & /CAS at VIH		-20	20	µA
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V
VOH	Output High Voltage	IOH = -5.0mA		2.4	-	V

NOTE

1. ICC1, ICC3, ICC4 and ICC6 depend on output loading and cycle rates(tRC and tHPC).
2. Specified values are obtained with outputs unloaded.
3. ICC is specified as an average current. In ICC1, ICC3, ICC6, address can be changed only once while /RAS=VIL. In ICC4, address can be changed maximum once while /CAS=VIH within one EDO mode cycle time tHPC.
4. Only /RAS(max.) = 1µs is applied to refresh of battery backup but tRAS(max.) = 10µs is to applied to normal functional operation.
5. ICC5(max.) = 6.4mA, ICC7 and ICC8 are applied to SL-part only.

AC CHARACTERISTICS

(T_A=0°C to 70°C, VCC=5V ± 10% and VSS=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM564224A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	150	-	175	-	195	-	ns	20
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	2
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	75	-	88	-	103	-	ns	2,20
5	tRAC	Access Time from /RAS	-	60	-	70	-	80	ns	5,6,7
6	tCAC	Access Time from /CAS	-	20	-	25	-	25	ns	5,6,20
7	tAA	Access Time from Column Address	-	35	-	40	-	45	ns	5,7,20
8	tCPA	Access Time from Column Precharge	-	40	-	40	-	45	ns	5,20
9	tCLZ	/CAS to Output Low Impedance	5	-	5	-	5	-	ns	5,20
10	tCEZ	Out Buffer Turn-Off Delay Time from /CAS	8	20	8	20	8	20	ns	8,12,20
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	/RAS Hold Time	18	-	20	-	25	-	ns	20
16	tCSH	/CAS Hold Time	38	-	48	-	58	-	ns	20
17	tCAS	/CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	/RAS to /CAS Delay Time	18	40	18	45	18	55	ns	6,20
19	tRAD	/RAS to Column Address Delay Time	13	25	13	30	13	35	ns	7,20
20	tCRP	/CAS to /RAS Precharge Time	10	-	10	-	10	-	ns	20
21	tCP	/CAS Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	5	-	5	-	5	-	ns	20
23	tRAH	Row Address Hold Time	8	-	8	-	8	-	ns	20
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tRAL	Column Address to /RAS Lead Time	35	-	40	-	45	-	ns	20
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	9
29	tRRH	Read Command Hold Time Referenced to /RAS	-2	-	-2	-	-2	-	ns	9,20
30	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
31	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
32	tRWL	Write Command to /RAS Lead Time	20	-	20	-	20	-	ns	20
33	tCWL	Write Command to /CAS Lead Time	13	-	15	-	20	-	ns	16

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HYM564224A X-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
34	tDS	Data-In Set-up Time	-2	-	-2	-	-2	-	ns	10,20
35	tDH	Data-In Hold Time	15	-	20	-	20	-	ns	10,20
36	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		Refresh Period (SL-part)	-	256	-	256	-	256	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	11
38	tCWD	/CAS to /WE Delay Time	37	-	45	-	45	-	ns	11,15
39	tRWD	/RAS to /WE Delay Time	78	-	93	-	103	-	ns	11,20
40	tAWD	Column Address to /WE Delay Time	50	-	60	-	65	-	ns	11
41	tCSR	/CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	17,20
42	tCHR	/CAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	18,20
43	tRPC	/RAS to /CAS Precharge Time	3	-	3	-	3	-	ns	20
44	tCPT	/CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	14
45	tROH	/RAS Hold Time Reference to /OE	15	-	15	-	15	-	ns	20
46	tOEA	/OE Access Time	-	20	-	25	-	25	ns	20
47	tOED	/OE to Data Delay Time	20	-	25	-	25	-	ns	20
48	tOEZ	Output Buffer Turn Off Delay Time from /OE	5	20	5	20	5	20	ns	8,20
49	tOEH	/OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	55	-	65	-	75	-	ns	11
51	tRHCP	/RAS Hold Time from /CAS Precharge	42	-	42	-	52	-	ns	20
52	tWRP	/WE to /RAS Precharge Time(CBR cycle)	12	-	12	-	12	-	ns	20
53	tWRH	/WE to /RAS Hold Time (CBR cycle)	8	-	8	-	8	-	ns	20
54	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	µs	
55	tRPS	/RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
56	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	
57	tDOH	Output Data Hold Time	10	-	10	-	10	-	ns	20
58	tREZ	Output Buffer Turn Off Delay from /RAS	3	15	3	15	3	15	ns	
59	tWEZ	Output Buffer Turn Off Delay from /WE	3	20	3	20	3	20	ns	20
60	tWED	/WE to Data Delay Time	20	-	20	-	20	-	ns	20
61	tOEP	/OE Precharge Time	5	-	5	-	5	-	ns	
62	tWPE	/WE Pulse Width (EDO cycle)	5	-	5	-	5	-	ns	
63	tOCH	/OE to /CAS Hold Time	5	-	5	-	5	-	ns	
64	tCHO	/CAS Hold Time to /OE	5	-	5	-	5	-	ns	

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. tASC ≥ tCP(min.), assume tT=2ns
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70°C) is assured.
5. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2TTL loads and 100pF.
6. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC
7. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA
8. tCEZ(max.), tOEZ(max.), tREZ(max.) and tWEZ(max.) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
9. Either tRCH or tRRH must be satisfied for a read cycle..
10. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
11. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ¡ ÃWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tCWD ≥ tCWD(min.), tRWD ≥ tRWD(min.) and tCPWD ≥ tCPWD(min.), then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
12. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going. If /CAS goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.
13. tASC and tCAH are referred to the earlier /CAS falling edge
14. tCP and tCPT are measured when both /LCAS and /UCAS are high state
15. tCWD is referred to the later /CAS falling dege at Read-Modify-Write cycle.
16. tCWL must be satisfied by both /LCAS and /UCAS for 16-bit access cycles.
17. tCSR is referred to the earlier /CAS falling low before /RAS transition low.
18. tCHR is referred to the later /CAS rising high after /RAS transition low.
19. tDS, tDH is independently specified for lower byte byte DQ(0-7), upper byte DQ(8-15).
20. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

CAPACITANCE

(T_A=25°C, VCC=5V ± 10%, VSS=0V and f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0~A9,B0)	-	13	pF
CIN2	Input Capacitance (/RAS0~/RAS3)	-	38	pF
CIN3	Input Capacitance (/CAS0~/CAS7, /WE0, /WE2, /OE0, /OE2)	-	13	pF
CDQ	Data Input /Output Capacitance (DQ0 - DQ63)	-	13	pF

PACKAGE INFORMATION

168 pin Buffered Dual In-line Memory Module