DATA SHEET

TZA3040
Gigabit Ethernet/Fibre Channel optical receiver

Objective specification
File under Integrated Circuits, IC19

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Philips
Semiconductors

PHILIPS

Gigabit Ethernet/Fibre Channel optical receiver TZA3040

FEATURES

- Equivalent input noise, typically 6.6 pA/√Hz
- Wide dynamic range, typically 2 μA to 1.5 mA
- Differential transimpedance of 1.1 MΩ
- On-chip Automatic Gain Control (AGC)
- Positive Emitter Coupled Logic (PECL) or Current-Mode Logic (CML) compatible data outputs
- Loss Of Signal (LOS) detection
- LOS threshold level can be adjusted using a single external resistor
- On-chip DC offset compensation
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode.

APPLICATIONS

- Digital fibre optic receiver in short, medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

GENERAL DESCRIPTION

The TZA3040 optical receiver is a high speed transimpedance amplifier with AGC plus a limiting amplifier designed to be used in Gigabit Ethernet/Fibre Channel applications. The TZA3040 amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3040HL	LQFP32	plastic low profile quad flat package; 32 leads; body 5 × 5 × 1.4 mm	SOT401-1
TZA3040U	–	naked die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

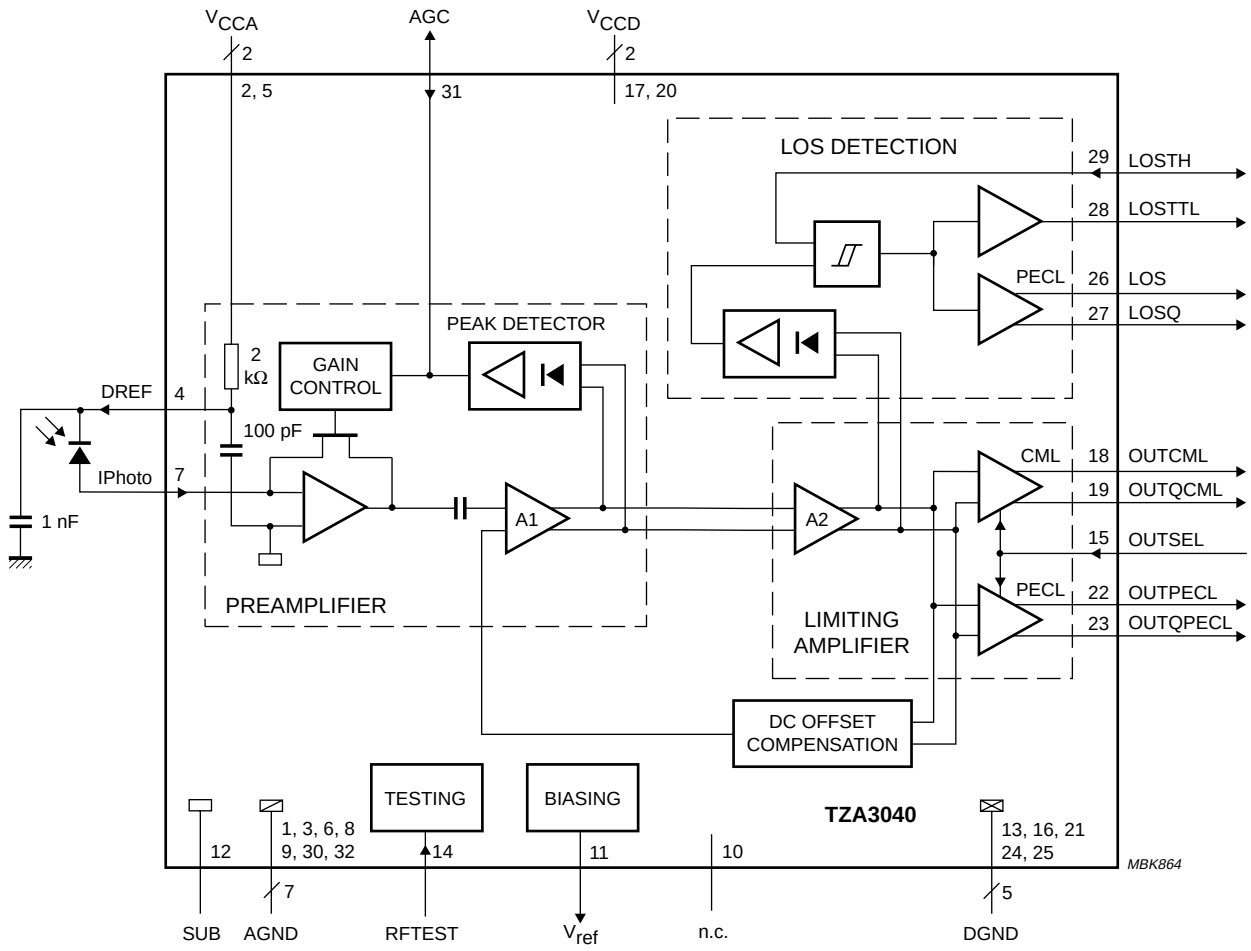


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
AGND	1	ground	analog ground
V_{CCA}	2	supply	analog supply voltage
AGND	3	ground	analog ground
DREF	4	analog output	bias voltage for PIN diode (V_{CCA}); cathode should be connected to this pin
V_{CCA}	5	supply	analog supply voltage
AGND	6	ground	analog ground
IPhoto	7	analog input	current input; connect the anode of PIN diode to this pin; DC bias level is 822 mV, one diode voltage above ground
AGND	8	ground	analog ground
AGND	9	ground	analog ground
n.c.	10	–	not connected
V_{ref}	11	analog output	band gap reference voltage; nominal value approximately 1.2 V
SUB	12	substrate	substrate pin; to be connected to AGND
DGND	13	ground	digital ground
RFTEST	14	analog input	test pin; not connected; not used in application
OUTSEL	15	CMOS input	output select pin; when OUTSEL is HIGH, CML data outputs are active and PECL data outputs are disabled; OUTSEL is pulled LOW if left unconnected, PECL data outputs will then be active and CML data outputs disabled
DGND	16	ground	digital ground
V_{CCD}	17	supply	digital supply voltage
OUTCML	18	CML output	CML data output; OUTCML goes HIGH when current flows into IPhoto (pin 7)
OUTQCML	19	CML output	CML compliment of OUTCML (pin 18)
V_{CCD}	20	supply	digital supply voltage
DGND	21	ground	digital ground
OUTPECL	22	PECL output	PECL data output; OUTPECL goes HIGH when current flows into IPhoto (pin 7)
OUTQPECL	23	PECL output	PECL compliment of OUTPECL (pin 22)
DGND	24	ground	digital ground
DGND	25	ground	digital ground
LOS	26	PECL output	PECL compatible LOS detection pin; LOS output is HIGH when the input signal is below the user programmable threshold level
LOSQ	27	PECL output	PECL compliment of LOS (pin 26)
LOSTTL	28	TTL output	TTL compatible LOS detection pin; the LOSTTL output is HIGH when the input signal is below the user programmable threshold level
LOSTH	29	analog I/O	pin for setting input threshold level; nominal DC voltage is V_{CCA} – 1.5 V; threshold level set by connecting an external resistor between LOSTH and V_{CCA} or by forcing a current into LOSTH; default value for this resistor is 39 kΩ
AGND	30	ground	analog ground
AGC	31	analog I/O	AGC monitor voltage; the internal AGC circuit can be disabled by applying an external voltage to this pin
AGND	32	ground	analog ground

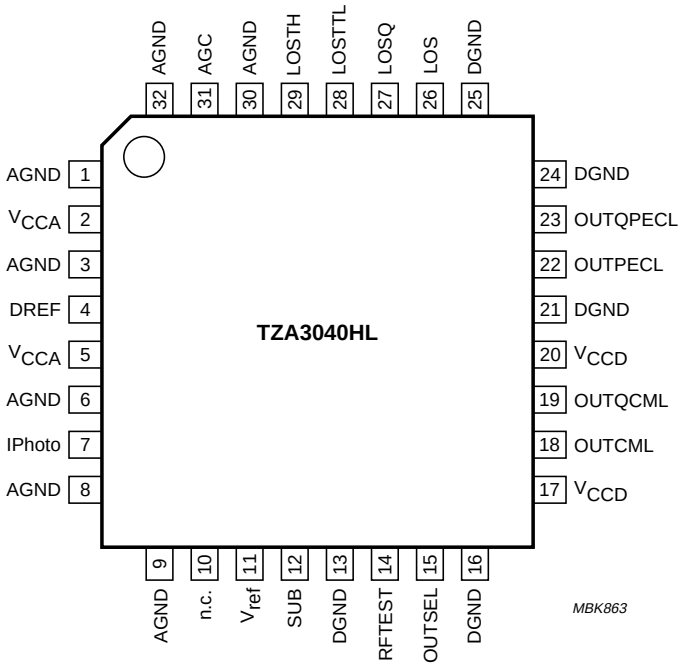


Fig.2 Pin configuration.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES(1)	
		x	y
AGND	1	102	1251
V_{CCA}	2	102	1111
AGND	3	102	971
DREF	4	102	814
V_{CCA}	5	102	674
AGND	6	102	534
IPhoto	7	102	395
AGND	8	102	254
AGND	9	243	105
n.c.	10	383	105
V_{ref}	11	523	105
SUB	12	663	105
DGND	13	803	105
RFTEST	14	943	105
OUTSEL	15	1100	105
DGND	16	1257	105
V_{CCD}	17	1398	263
OUTCML	18	1398	403

SYMBOL	PAD	COORDINATES(1)	
		x	y
OUTQCML	19	1398	543
V_{CCD}	20	1398	683
DGND	21	1398	823
OUTPECL	22	1398	963
OUTQPECL	23	1398	1103
DGND	24	1398	1243
DGND	25	1283	1400
LOS	26	1143	1400
LOSQ	27	986	1400
LOSTTL	28	829	1400
LOSTH	29	671	1400
AGND	30	514	1400
AGC	31	357	1400
AGND	32	217	1400

Note

1. All coordinates (µm) are measured with respect to the bottom left-hand corner of the die.

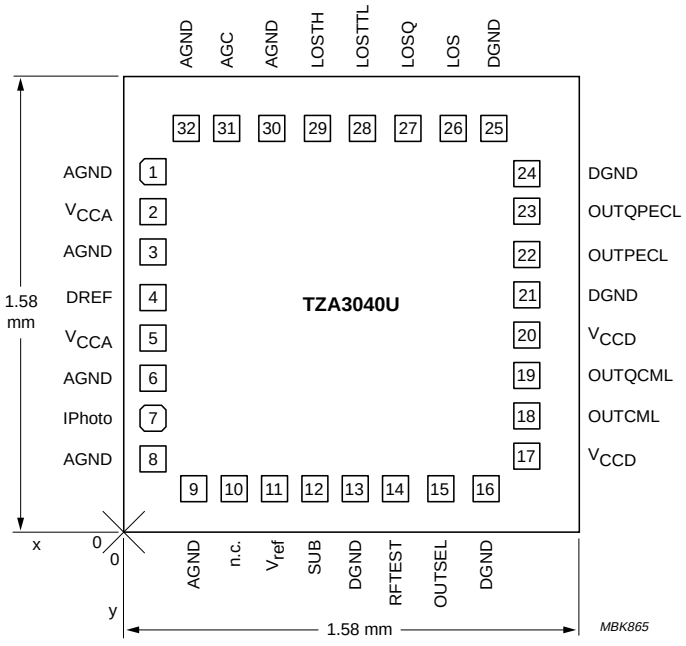


Fig.3 Bonding pad locations of TZA3040U.

FUNCTIONAL DESCRIPTION

The TZA3040 contains four functional blocks:

- Preamplifier input stage
- Limiting amplifier stage
- Offset compensation loop
- Loss of signal detection unit.

Preamplifier

The preamplifier provides low-noise amplification of the current generated by a photodiode connected to pin IPhoto.

A differential amplifier converts the output of the preamplifier to a differential voltage. An AGC loop increases the dynamic range of the receiver by reducing the feedback resistance of the preamplifier. The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not needed for AGC. The AGC voltage can be monitored at pin AGC. This pin can be left unconnected for normal operation. It can also be used to force an external AGC voltage. If pin AGC is connected to AGND, the internal AGC loop is disabled and the receiver gain is at a maximum. In this case, the maximum input current is approximately 75 μA.

Limiting amplifier

A limiting amplifier boosts the signal up to PECL levels. The output can be either CML or PECL compatible, selected by means of pin OUTSEL. When OUTSEL is HIGH, the CML data outputs are active and the PECL data outputs are disabled. If OUTSEL is left unconnected, it is pulled LOW and the PECL data outputs are active while CML data outputs are disabled.

The logic level symbol definitions for CML and PECL are shown in Fig.4.

The CML and PECL output circuits are given in Fig.5.

Offset compensation loop

A control loop connected between the limiting amplifier output and the differential amplifier input cancels the DC offset. The loop bandwidth is fixed internally at 30 kHz.

Loss Of Signal (LOS) detection

The LOS section detects an input signal level below a fixed threshold. The threshold is determined by the current through pin LOSTH. If this current is increased, the threshold level will rise. An external resistor connected between pin LOSTH and V_{CCA} can be used, or a current can be forced into pin LOSTH. The default value for the external resistor is 39 kΩ. In this case, the current through pin LOSTH will be approximately 38.5 μA since the voltage at pin LOSTH is regulated at 1.5 V below the supply voltage. This threshold corresponds to an input current of 2.1 μA. The ratio of LOSTH current to input current is thus approximately 18 : 1. When the input signal level falls below this threshold, the LOS (PECL compatible) and LOSTTL (TTL compatible) outputs go HIGH. The hysteresis is fixed internally at 3 dB. Response time is typically less than 20 μs.

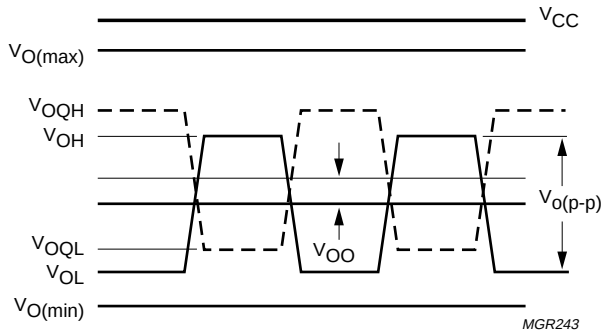
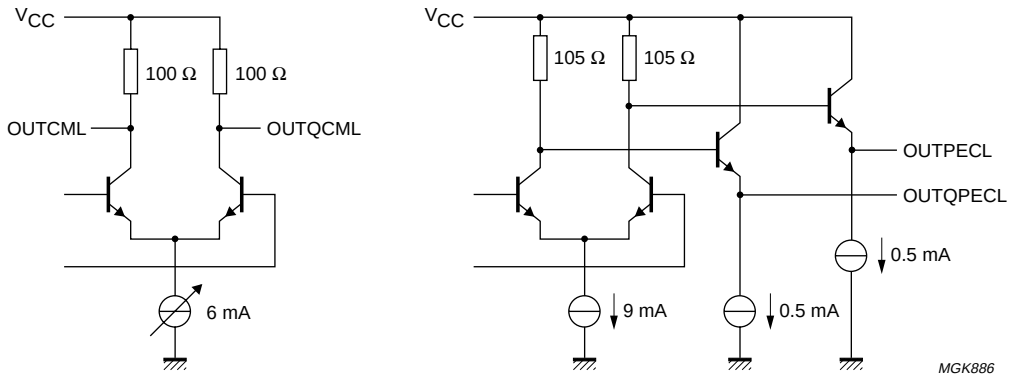


Fig.4 Logic level symbol definitions for CML and PECL.



a. CML. b. PECL.

Fig.5 Output circuits.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6	V
V_n	DC voltage			
	pin 7: IPhoto	–0.5	+1	V
	pin 14: RFTEST	–0.5	V_{CC} + 0.5	V
	pins 22, 23, 26 and 27: OUTPECL, OUTQPECL, LOS and LOSQ	V_{CC} – 2	V_{CC} + 0.5	V
	pins 18 and 19: OUTCML and OUTQCML	V_{CC} – 2	V_{CC} + 0.5	V
	pin 29: LOSTH	–0.5	V_{CC} + 0.5	V
	pin 10: n.c.	–0.5	V_{CC} + 0.5	V
	pin 31: AGC	–0.5	V_{CC} + 0.5	V
	pin 11: V_{ref}	–0.5	+3.2	V
	pin 4: DREF	–0.5	V_{CC} + 0.5	V
	pin 15: OUTSEL	–0.5	V_{CC} + 0.5	V
	pin 28: LOSTTL	–0.5	V_{CC} + 0.5	V
I_n	DC current			
	pin 7: IPhoto	–2.5	+2.5	mA
	pin 14: RFTEST	–2	+2	mA
	pins 22, 23, 26 and 27: OUTPECL, OUTQPECL, LOS and LOSQ	–25	+10	mA
	pins 18 and 19: OUTCML and OUTQCML	–15	+15	mA
	pin 29: LOSTH	–2	+2	mA
	pin 10: n.c.	–1	+1	mA
	pin 31: AGC	–0.2	+0.2	mA
	pin 11: V_{ref}	–2	+2.5	mA
	pin 4: DREF	–2.5	+2.5	mA
	pin 15: OUTSEL	–0.5	+0.5	mA
	pin 28: LOSTTL	–16	+16	mA
P_{tot}	total power dissipation	–	600	mW
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	operating ambient temperature	–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	tbf	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	tbf	K/W

CHARACTERISTICS

For typical values T_{amb} = 25 °C and V_{CC} = 5 V; minimum and maximum values are valid over the entire ambient temperature range and process spread.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3	5	5.5	V
I_{CCD}	digital supply current	note 1	tbf	22	tbf	mA
		note 2	–	48	–	mA
		note 3	tbf	24	tbf	mA
I_{CCA}	analog supply current		tbf	44	tbf	mA
P_{tot}	total power dissipation		–	–	550	mW
T_j	junction temperature		–40	–	+110	°C
T_{amb}	operating ambient temperature		–40	+25	+85	°C
R_{tr}	small-signal transresistance of the receiver	measured differentially				
		PECL outputs	–	1150	–	kΩ
		CML outputs	–	812	–	kΩ
$f_{-3dB(h)}$	high frequency –3 dB point	V_{CC} = 5V; C_i = 1pF	–	900	–	MHz
		V_{CC} = 3.3V; C_i = 1pF	–	800	–	MHz
$f_{-3dB(l)}$	low frequency –3 dB point		20	30	40	kHz
$I_{n(tot)}$	total integrated RMS noise current over bandwidth	referenced to input; C_i = 1.2 pF; note 4				
		Δf = 800 MHz; V_{CC} = 3.3 V	–	192	–	nA
		Δf = 900 MHz; V_{CC} = 5.0 V	–	218	–	nA
PSRR	power supply rejection ratio	measured differentially; note 5				
		f = 100 kHz to 1 MHz	–	7	–	µA/V
		f = 1 MHz to 100 MHz	–	13	–	µA/V
		f = 100 MHz to 1 GHz	–	70	–	µA/V
$\Delta R_{tr}/\Delta t$	AGC loop constant		–	1	–	dB/ms
Input: IPhoto						
$V_{bias(IPhoto)}$	input bias voltage		650	822	957	mV
$I_{i(IPhoto)(p-p)}$	input current (peak-to-peak value)	V_{CC} = 5 V	–2000	+4	+2000	µA
		V_{CC} = 3.3 V	–1000	+4	+1000	µA
PECL outputs: OUTPECL and OUTQPECL						
V_{OH}	HIGH-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1100	–	V_{CC} – 900	mV
V_{OL}	LOW-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1840	–	V_{CC} – 1620	mV
V_{OO}	output offset voltage	measured differentially	–10	–	+10	mV
t_r	rise time	20% to 80%	–	150	200	ps
t_f	fall time	80% to 20%	–	140	200	ps

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PECL outputs: LOS and LOSQ						
V_{OH}	HIGH-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1100	–	V_{CC} – 900	mV
V_{OL}	LOW-level output voltage	50 Ω to V_{CC} – 2 V	V_{CC} – 1840	–	V_{CC} – 1620	mV
V_{OO}	output offset voltage	measured differentially	–10	–	+10	mV
t_r	rise time	20% to 80%	–	–	600	ns
t_f	fall time	80% to 20%	–	–	200	ns
CML outputs: OUTCML and OUTQCML						
V_O	output voltage	measured single-ended; 50 Ω to V_{CC}	V_{CC} – 260	–	V_{CC}	mV
$V_{o(se)(p-p)}$	output voltage single-ended (peak-to-peak value)	50 Ω to V_{CC}	150	200	260	mV
V_{OO}	output offset voltage	measured differentially; 50 Ω to V_{CC}	–10	–	+10	mV
R_o	output resistance	measured single-ended	80	100	120	Ω
t_r	rise time	20% to 80%; R_L = 50 Ω; C_L = 1 pF	–	92	–	ps
t_f	fall time	80% to 20%; R_L = 50 Ω; C_L = 1 pF	–	62	–	ps
CMOS input: OUTSEL						
V_{IL}	LOW-level input voltage		–	0.4	0.8	V
V_{IH}	HIGH-level input voltage		V_{CC} – 1	V_{CC} – 0.5	–	V
CMOS output: LOSTTL						
V_{OL}	LOW-level output voltage			–	0.2	V
V_{OH}	HIGH-level output voltage		V_{CC} – 0.2	–	V_{CC}	V

Notes

1. OUTPECL, OUTQPECL, OUTCML, OUTQCML, LOS and LOSQ outputs are left unconnected. OUTPECL and OUTQPECL outputs are active.
2. OUTPECL and OUTQPECL outputs are terminated with 50 Ω to V_T. V_T is an external termination voltage for PECL outputs and is 2 V below the supply voltage. OUTCML, OUTQCML, LOS and LOSQ outputs are left unconnected.
3. OUTCML and OUTQCML outputs are terminated with 50 Ω to V_{CCD}; CML outputs are active. OUTPECL, OUTQPECL, LOS and LOSQ outputs are left unconnected.
4. All $I_{n(tot)}$ measurements were made with an input capacitance of C_i = 1.2 pF. This was comprised of 0.7 pF for the photodiode itself, with 0.3 pF allowed for the PCB layout and 0.2 pF intrinsic to the package.
5. PSRR is defined as the ratio of the equivalent current change at the input (ΔI_{IPhoto}) to a change in supply voltage:

   $$PSRR = \frac{\Delta I_{IPhoto}}{\Delta V_{CC}}$$

   For example, a 3 mV disturbance on V_{CC} at 1 MHz will typically generate the equivalent of 21 nA extra photodiode current. The external capacitor between DREF and GND has a large impact on PSRR. The specification is valid with an external capacitor of 1 nF.

APPLICATION INFORMATION

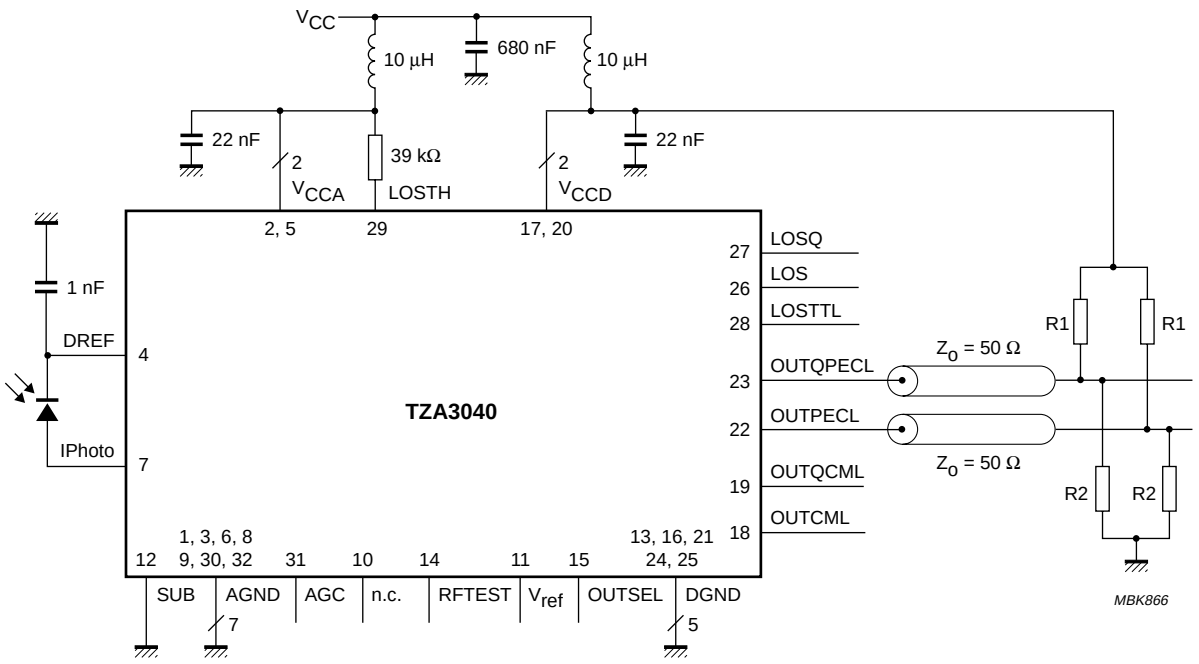


Fig.6 Application diagram: PECL data outputs active.

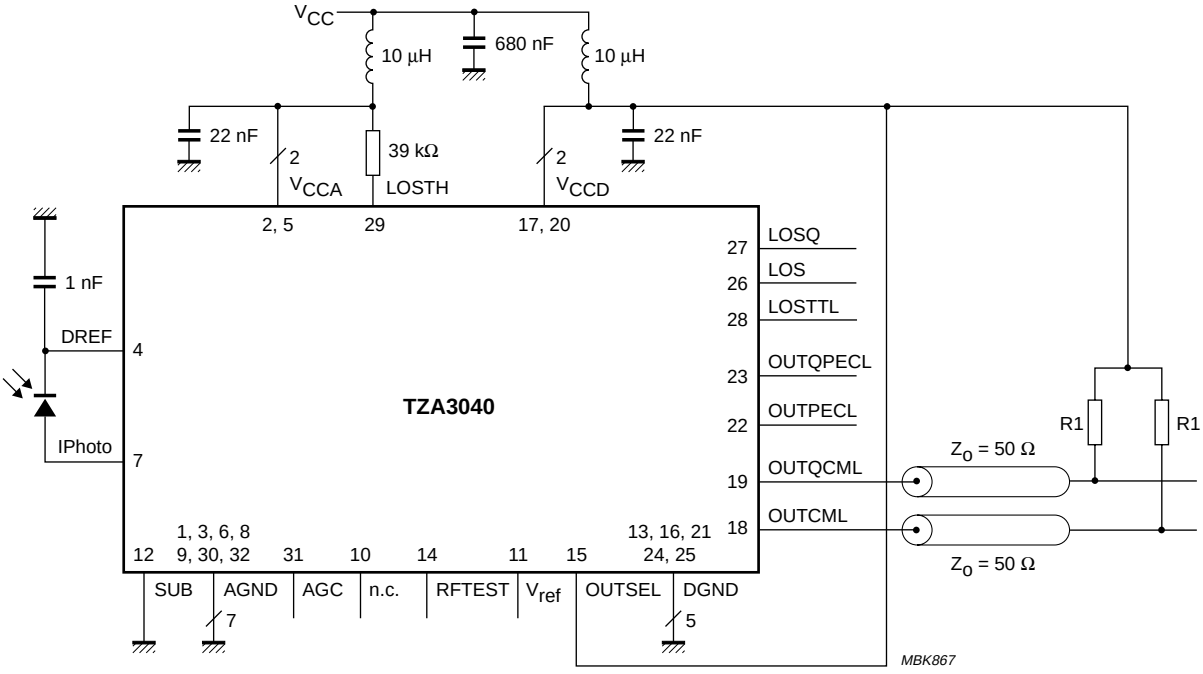


Fig.7 Application diagram: CML data outputs active.

PECL outputs: OUTPECL, OUTQPECL, LOS and LOSQ

PECL outputs can be terminated in different ways depending on the power supply voltage (see Fig.8).

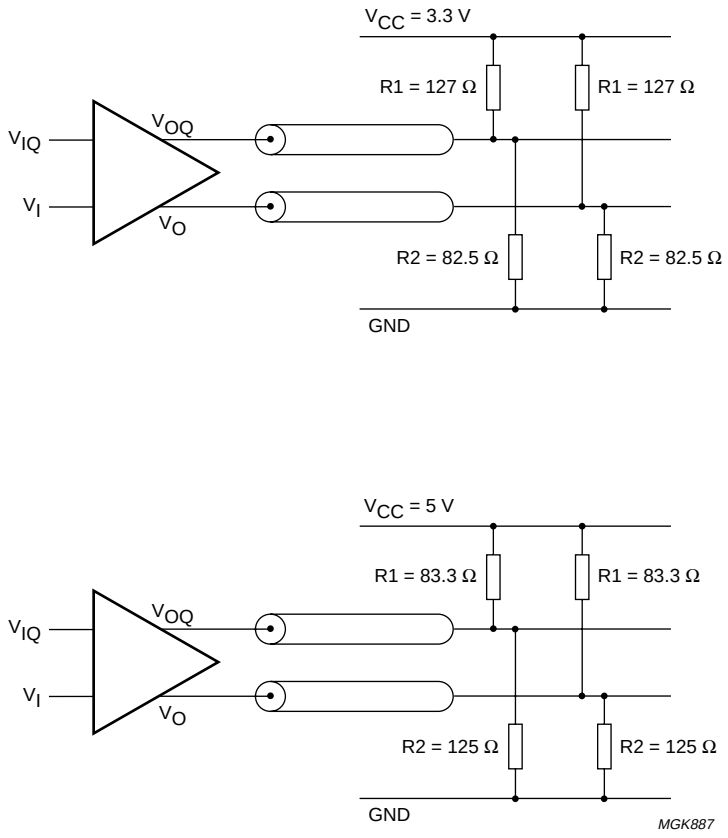


Fig.8 PECL termination schemes.

CML outputs: OUTCML and OUTQCML

The output impedance of the CML output driver is 100 Ω (see Fig.9), which doesn't match the characteristic impedance of the strip line. While this means that the reflections of some incident edges will arrive at the driver output on the PCB, this value was selected to reduce power dissipation inside the IC. The parallel combination of 100 Ω and 50 Ω (33 Ω) will generate a signal swing of 200 mV (peak-to-peak value, single-sided) with a tail current of 6 mA.

If the output impedance was 50 Ω rather than 100 Ω, an 8 mA tail current would be needed to generate the same voltage swing. This would increase power dissipation by 33%.

If necessary, the output impedance of the generator can be matched to the line impedance by connecting an external 100 Ω resistor in parallel with the output as shown in Fig.10. The magnitude of the output voltage swing will not change due to adaptive regulation. However, power dissipation will increase by 33%.

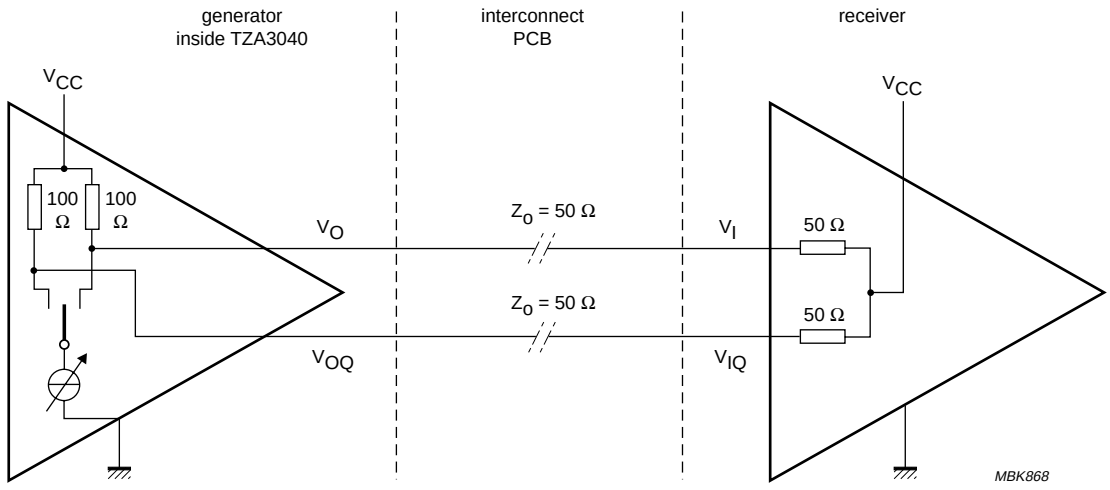


Fig.9 CML interface circuit without matched impedance; low power dissipation.

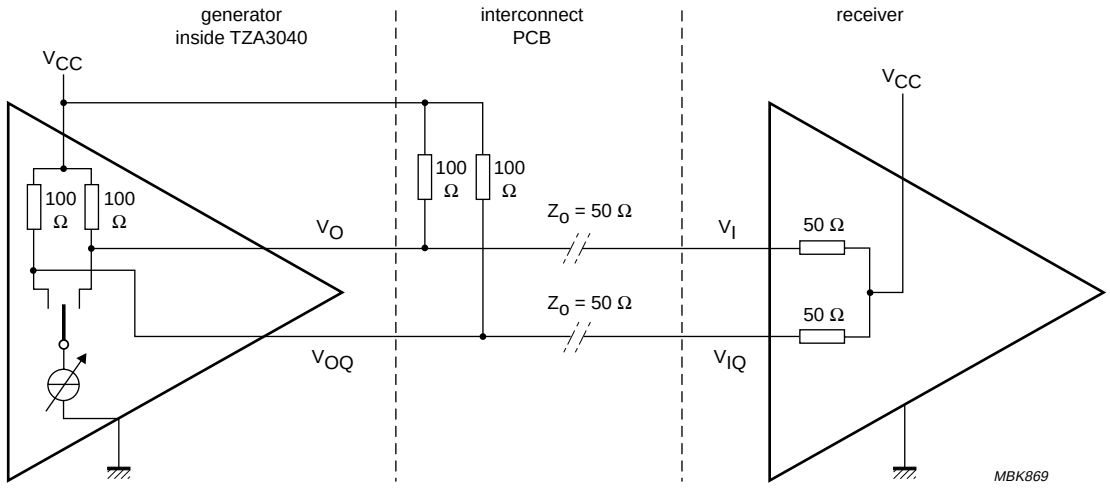
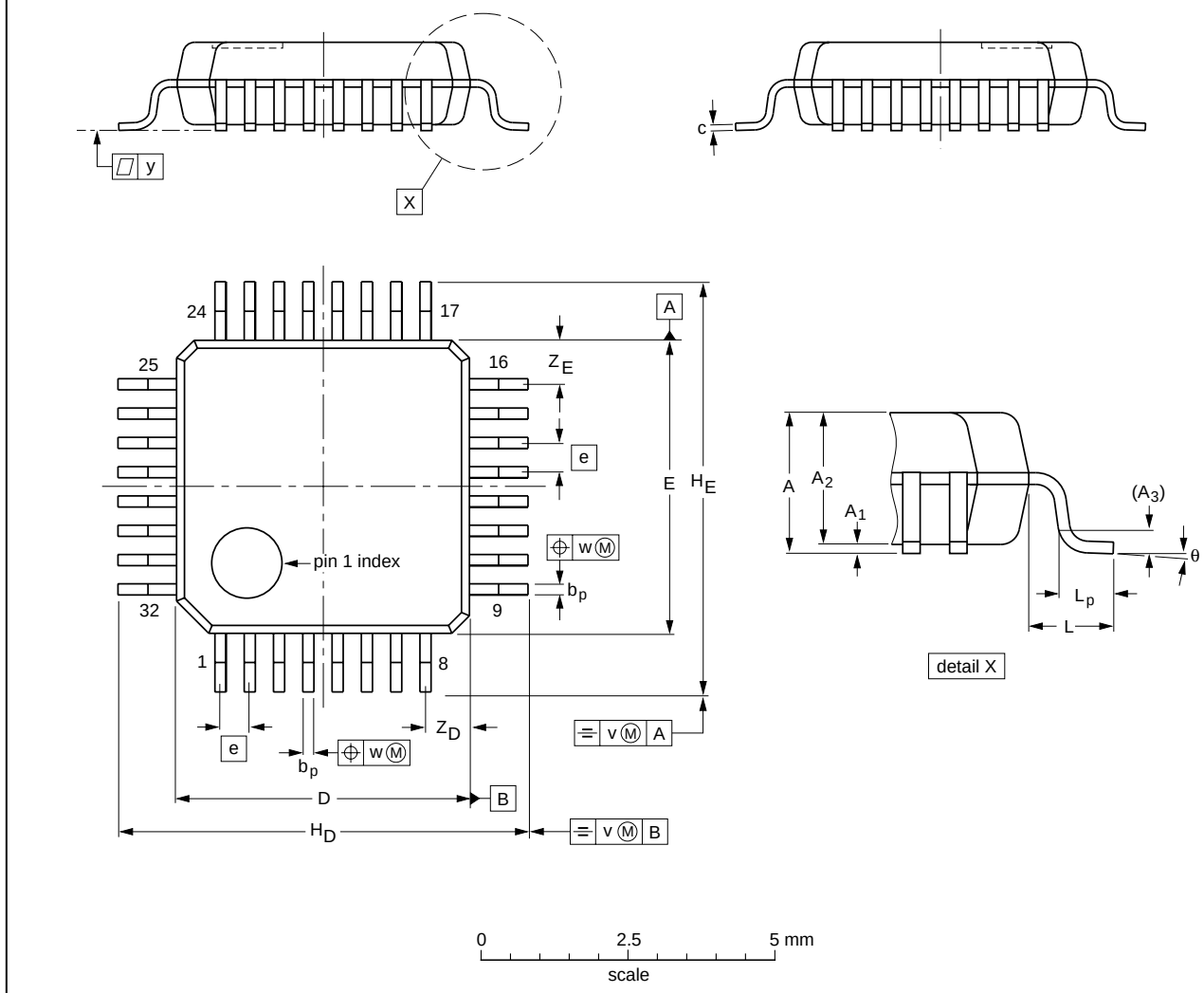


Fig.10 CML interface circuit with matched impedance; high power dissipation.

PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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