

# BUD42D

## High Speed, High Gain Bipolar NPN Transistor Integrating an Antisaturation Network and a Transient Voltage Suppression Capability

The BUD42D is a state-of-the-art bipolar transistor. Tight dynamic characteristics and lot to lot minimum spread make it ideally suitable for light ballast applications.

### Main Features:

- Free Wheeling Diode Built In
- Flat DC Current Gain
- Fast Switching Times and Tight Distribution
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads

### Two Versions:

- BUD42D-1: Case 369-07 for Insertion Mode
- BUD42D: Case 369A-13 for Surface Mount Mode

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	350	Vdc
Collector-Base Breakdown Voltage	$V_{CBO}$	650	Vdc
Collector-Emitter Breakdown Voltage	$V_{CES}$	650	Vdc
Emitter-Base Voltage	$V_{EBO}$	9	Vdc
Collector Current – Continuous	$I_C$	4.0	Adc
– Peak (Note 1)	$I_{CM}$	8.0	
Base Current – Continuous	$I_B$	1.0	Adc
– Peak (Note 1)	$I_{BM}$	2.0	
*Total Device Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	25	Watt
*Derate above $25^\circ\text{C}$		0.2	W/ $^\circ\text{C}$
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### TYPICAL GAIN

Typical Gain @ $I_C = 1\text{ A}, V_{CE} = 2\text{ V}$	$h_{FE}$	13	–
Typical Gain @ $I_C = 0.3\text{ A}, V_{CE} = 1\text{ V}$	$h_{FE}$	16	–

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	5.0	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 seconds	$T_L$	260	$^\circ\text{C}$

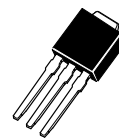
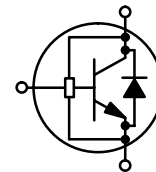
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%



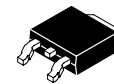
ON Semiconductor™

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**4 AMPERES  
650 VOLTS  
25 WATTS  
POWER TRANSISTOR**

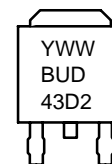
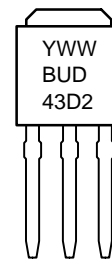


DPAK  
CASE 369  
STYLE 1



DPAK  
CASE 369A  
STYLE 1

### MARKING DIAGRAMS



Y = Year  
WW = Work Week  
BUD43D2 = Device Code

### ORDERING INFORMATION

Device	Package	Shipping
BUD42D	DPAK	75 Units/Rail
BUD42D-1	DPAK	75 Units/Rail

# BUD42D

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	350	430	–	Vdc	
Collector–Base Breakdown Voltage (I <sub>CBO</sub> = 1 mA)	V <sub>CBO</sub>	650	780	–	Vdc	
Emitter–Base Breakdown Voltage (I <sub>EBO</sub> = 1 mA)	V <sub>EBO</sub>	9.0	12	–	Vdc	
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	@ T <sub>C</sub> = 25°C	–	–	100	μAdc
		@ T <sub>C</sub> = 125°C	–	–	200	
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0)	I <sub>CES</sub>	@ T <sub>C</sub> = 25°C	–	–	10	μAdc
		@ T <sub>C</sub> = 125°C	–	–	200	
Emitter–Cutoff Current (V <sub>EB</sub> = 9 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	100	μAdc	

### ON CHARACTERISTICS

Base–Emitter Saturation Voltage (I <sub>C</sub> = 1 Adc, I <sub>B</sub> = 0.2 Adc)	V <sub>BE(sat)</sub>	–	0.85	1.2	Vdc
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 2 Adc, I <sub>B</sub> = 0.5 Adc)	V <sub>CE(sat)</sub>	–	0.2	1.0	Vdc
DC Current Gain (I <sub>C</sub> = 1 Adc, V <sub>CE</sub> = 2 Vdc) (I <sub>C</sub> = 2 Adc, V <sub>CE</sub> = 5 Vdc)	h <sub>FE</sub>	8.0	13	–	–
		10	12	–	

### DIODE CHARACTERISTICS

Forward Diode Voltage (I <sub>EC</sub> = 1.0 Adc)	V <sub>EC</sub>	–	0.9	1.5	V
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### SWITCHING CHARACTERISTICS: Resistive Load (D.C. ≤ 10%, Pulse Width = 40 μs)

Turn–Off Time (I <sub>C</sub> = 1.2 Adc, I <sub>B1</sub> = 0.4 A, I <sub>B2</sub> = 0.1 A, V <sub>CC</sub> = 300 V)	T <sub>off</sub>	4.6	–	6.55	μs
Fall Time (I <sub>C</sub> = 2.5 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.5 A, V <sub>CC</sub> = 150 V, V <sub>BE</sub> = –2 V)	T <sub>f</sub>	–	–	0.8	μs

### DYNAMIC SATURATION VOLTAGE

Dynamic Saturation Voltage: Determined 1 μs and 3 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub>	I <sub>C</sub> = 400 mA I <sub>B1</sub> = 40 mA V <sub>CC</sub> = 300 V	@ 1 μs	@ T <sub>C</sub> = 25°C	V <sub>CCE(dsat)</sub>	–	2.8	–	V
			@ T <sub>C</sub> = 125°C		–	3.2	–	
		@ 3 μs	@ T <sub>C</sub> = 25°C		–	0.75	–	
			@ T <sub>C</sub> = 125°C		–	1.3	–	
	I <sub>C</sub> = 1 A I <sub>B1</sub> = 200 mA V <sub>CC</sub> = 300 V	@ 1 μs	@ T <sub>C</sub> = 25°C		–	2.1	–	
			@ T <sub>C</sub> = 125°C		–	4.7	–	
		@ 3 μs	@ T <sub>C</sub> = 25°C		–	0.35	–	
			@ T <sub>C</sub> = 125°C		–	0.6	–	

TYPICAL STATIC CHARACTERISTICS

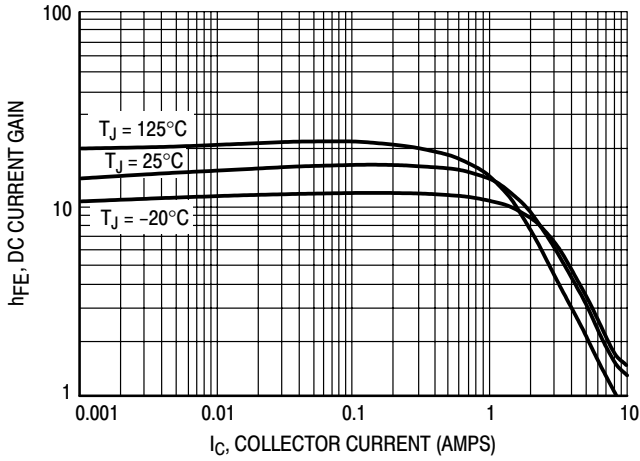


Figure 1. DC Current Gain @  $V_{CE} = 1\text{ V}$

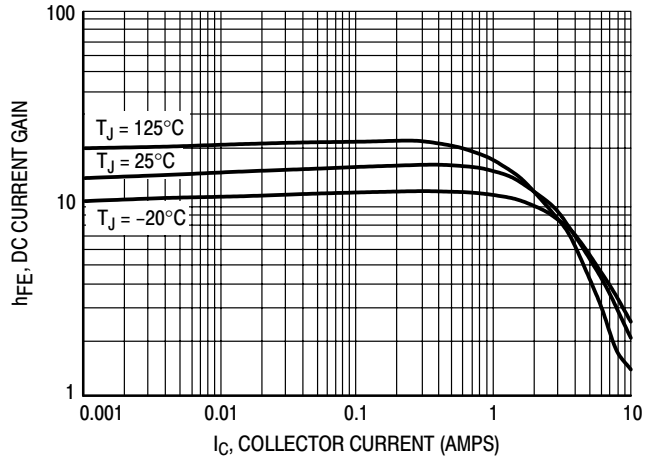


Figure 2. DC Current Gain @  $V_{CE} = 5\text{ V}$

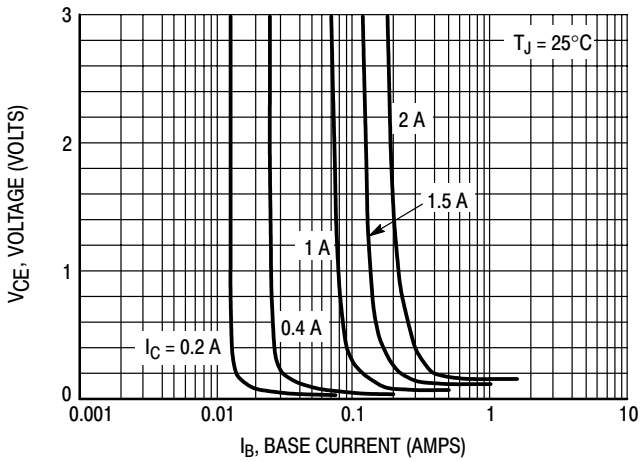


Figure 3. Collector Saturation Region

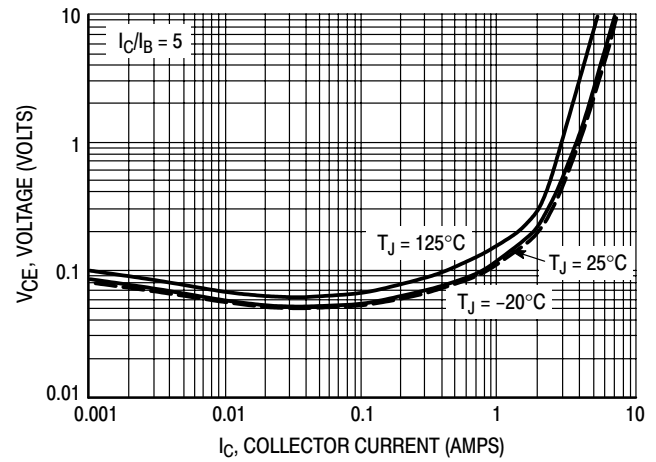


Figure 4. Collector-Emitter Saturation Voltage

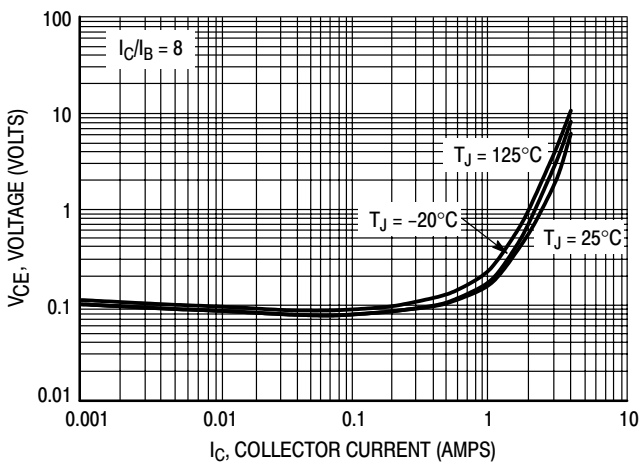


Figure 5. Collector-Emitter Saturation Voltage

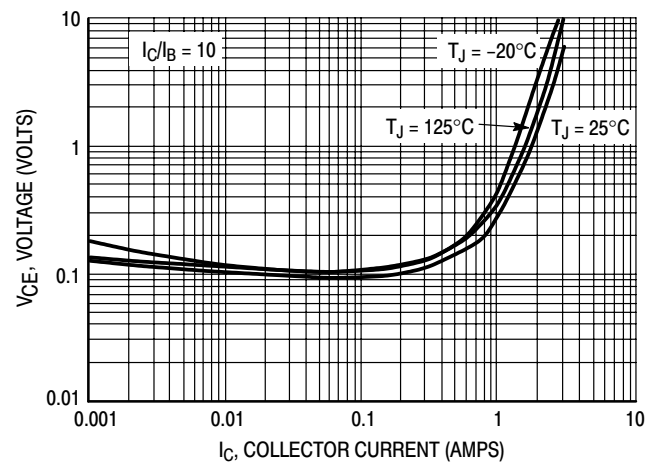


Figure 6. Collector-Emitter Saturation Voltage

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## TYPICAL STATIC CHARACTERISTICS

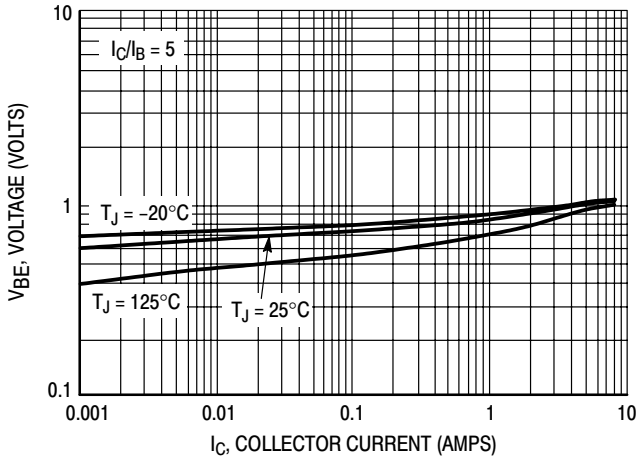


Figure 7. Base-Emitter Saturation Region

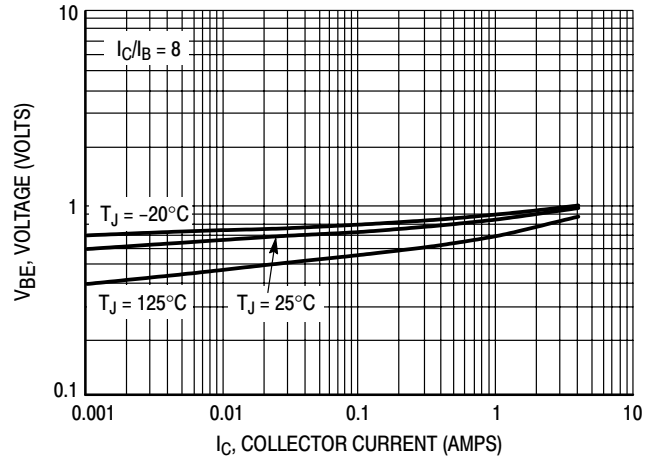


Figure 8. Base-Emitter Saturation Region

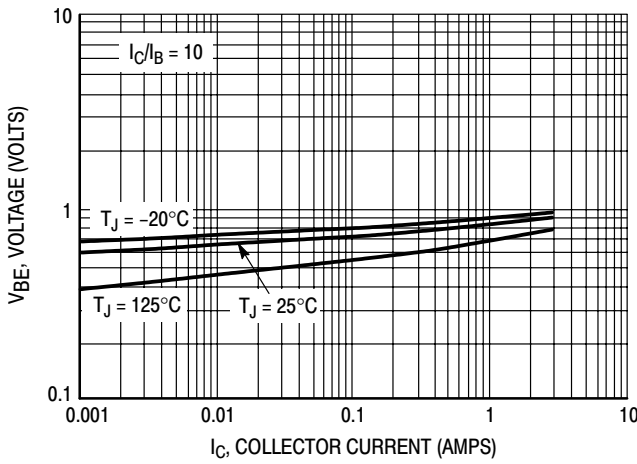


Figure 9. Base-Emitter Saturation Region

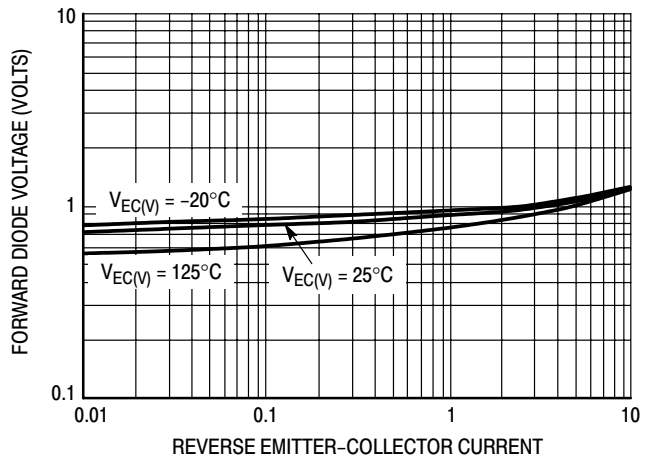


Figure 10. Forward Diode Voltage

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## TYPICAL SWITCHING CHARACTERISTICS

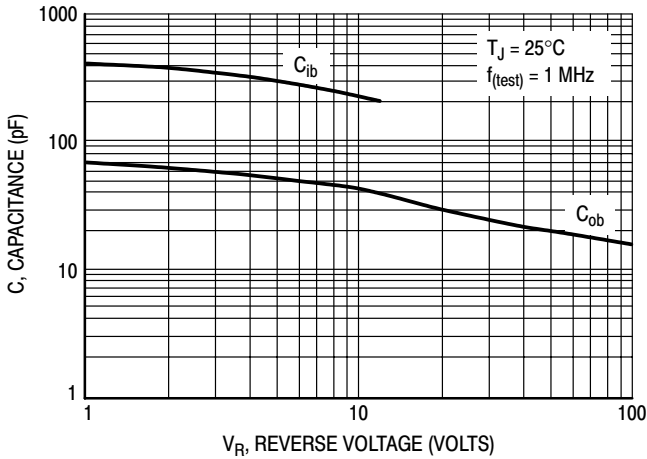


Figure 11. Capacitance

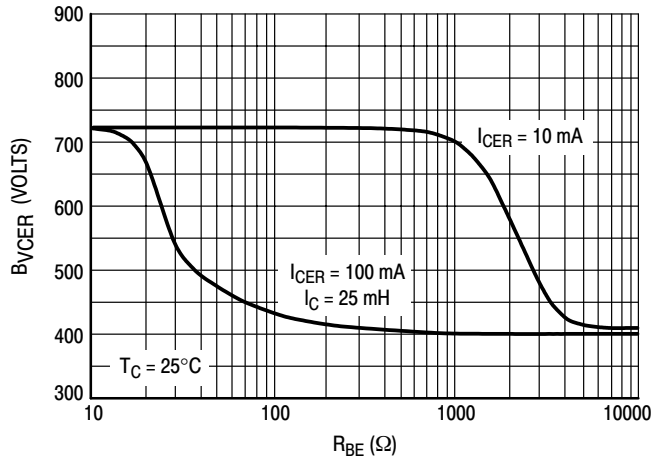


Figure 12.  $V_{BCE} = f(R_{BE})$

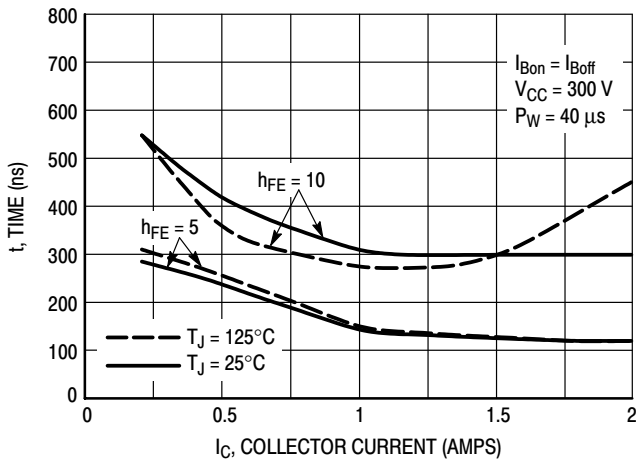


Figure 13. Resistive Switching,  $t_{on}$

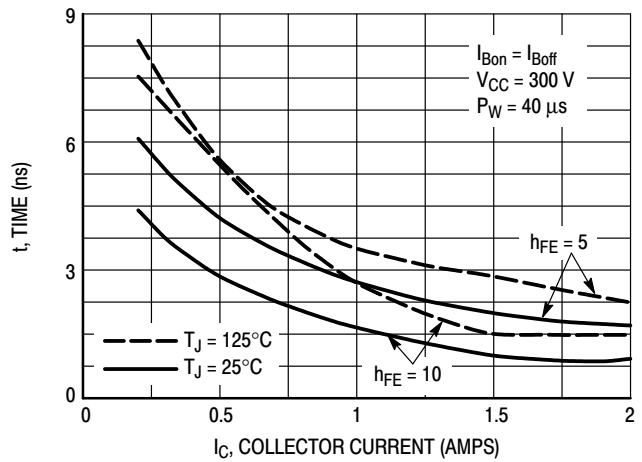


Figure 14. Resistive Switching,  $t_{off}$

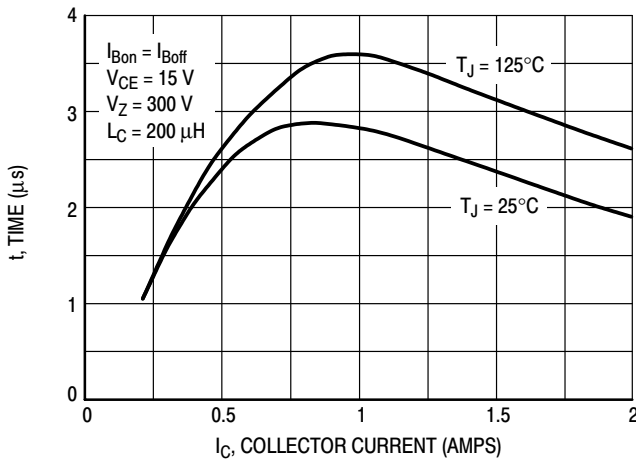


Figure 15. Inductive Storage Time,  $t_{si}$  @  $h_{FE} = 5$

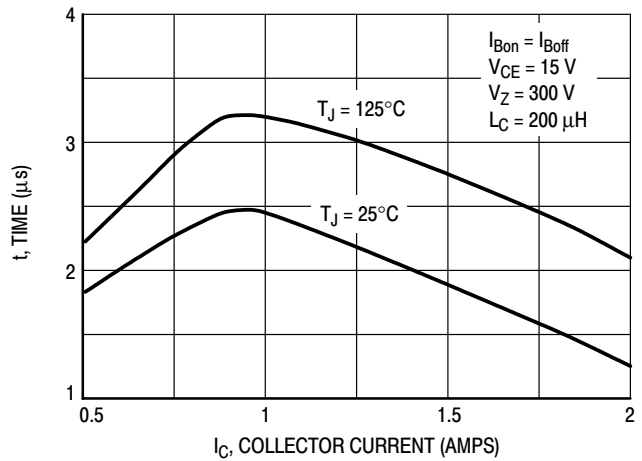


Figure 16. Inductive Storage Time,  $t_{si}$  @  $h_{FE} = 10$

TYPICAL SWITCHING CHARACTERISTICS

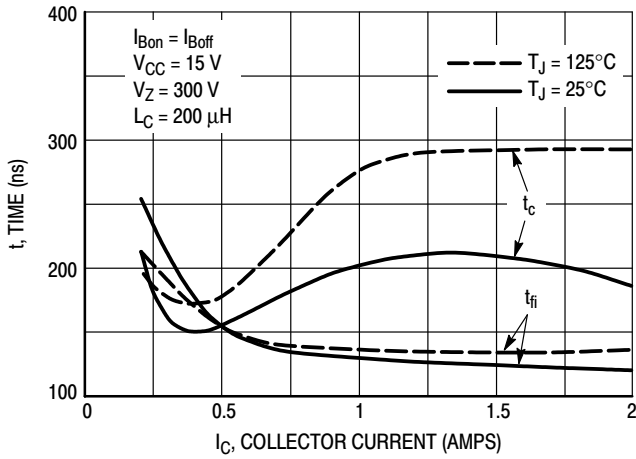


Figure 17. Inductive Fall and Cross Over Time,  $t_{fi}$  and  $t_c$  @  $h_{FE} = 5$

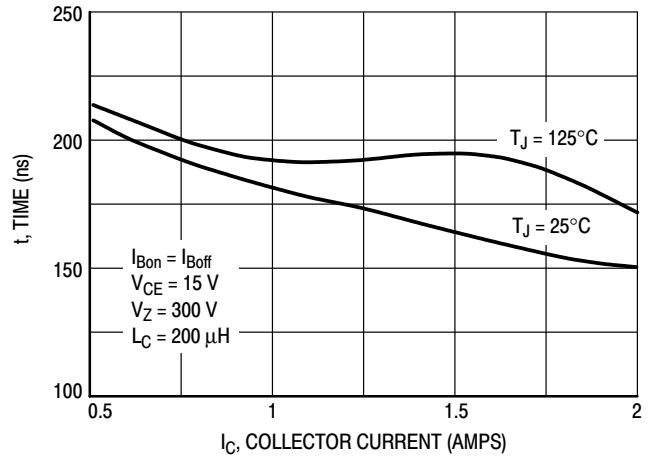


Figure 18. Inductive Fall Time,  $t_{fi}$  @  $h_{FE} = 10$

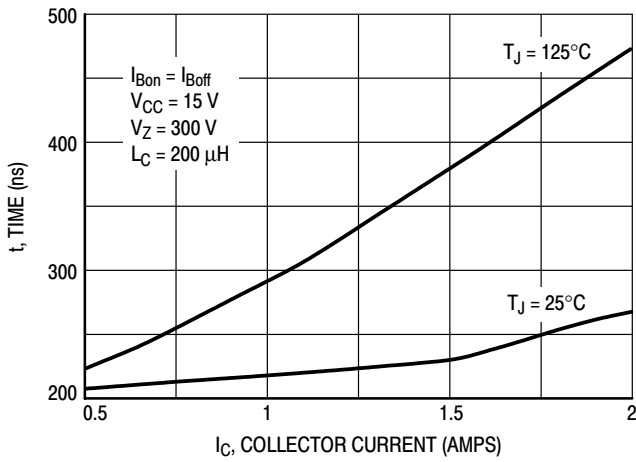


Figure 19. Inductive Cross Over Time,  $t_c$  @  $h_{FE} = 10$

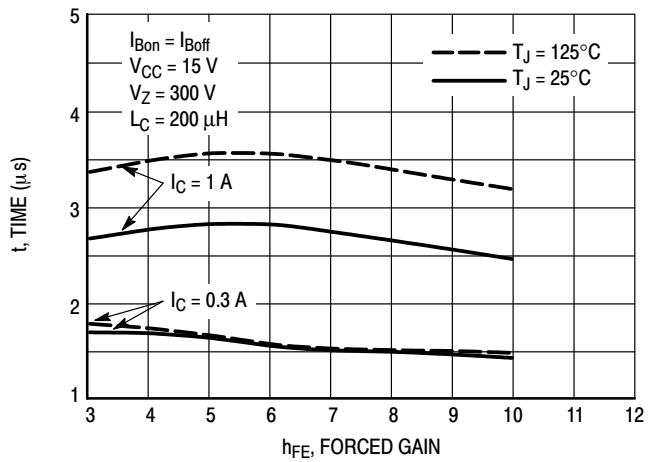


Figure 20. Inductive Storage Time,  $t_{si}$

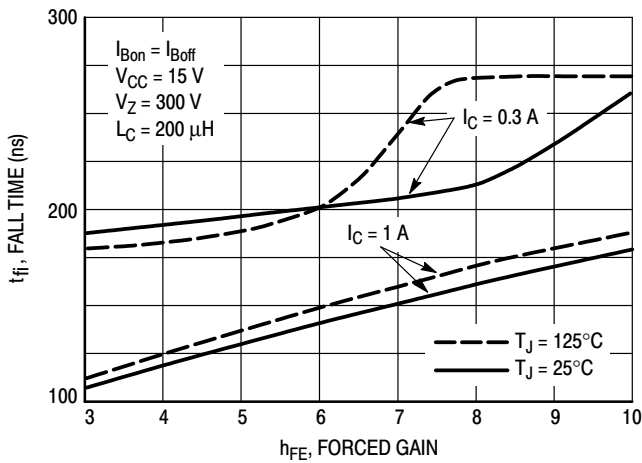


Figure 21. Inductive Fall Time,  $t_f$

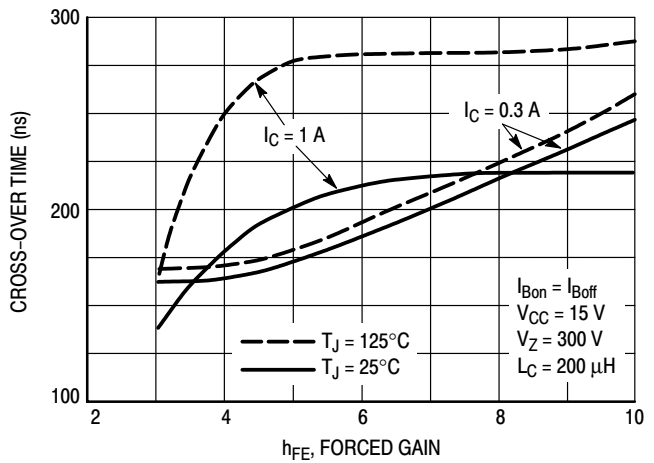


Figure 22. Inductive Cross Over Time,  $t_c$

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## TYPICAL SWITCHING CHARACTERISTICS

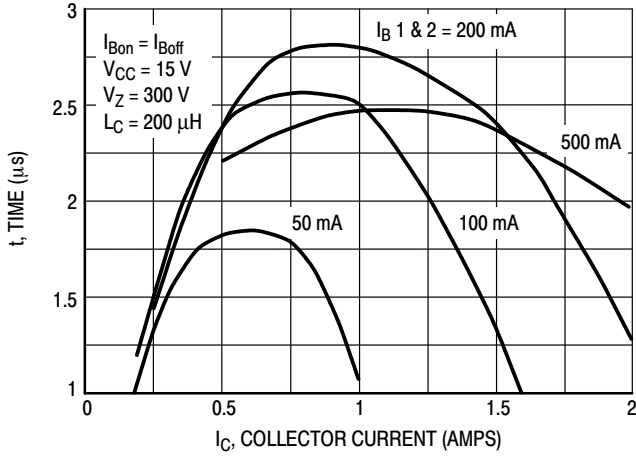


Figure 23. Inductive Storage Time,  $t_{si}$

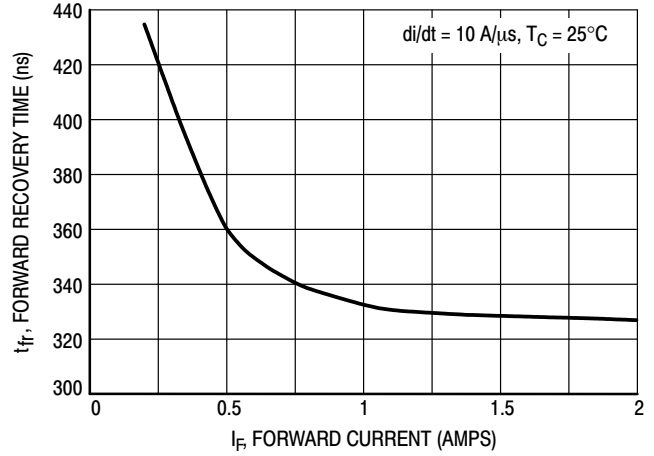


Figure 24. Forward Recovery Time,  $t_{fr}$

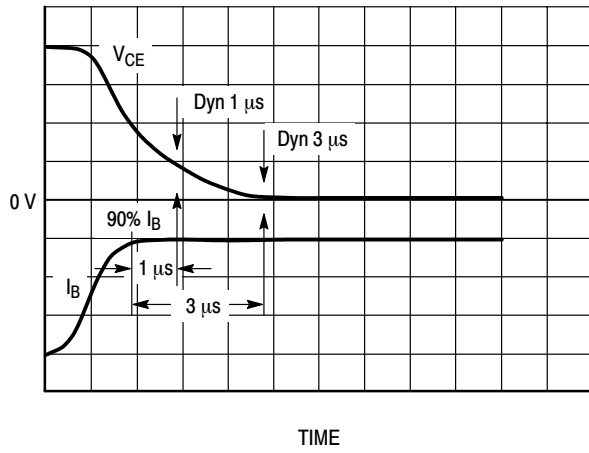


Figure 25. Dynamic Saturation Voltage Measurements

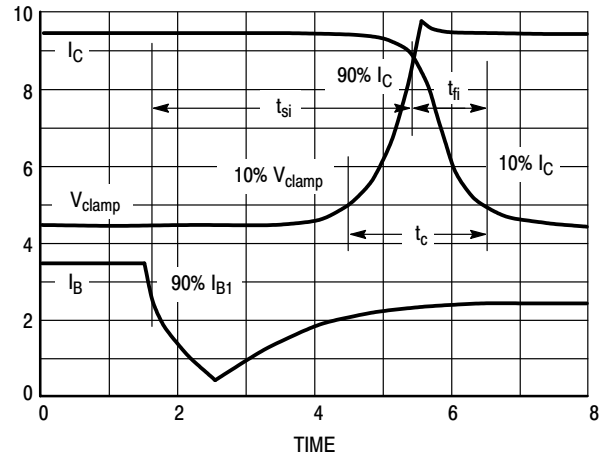
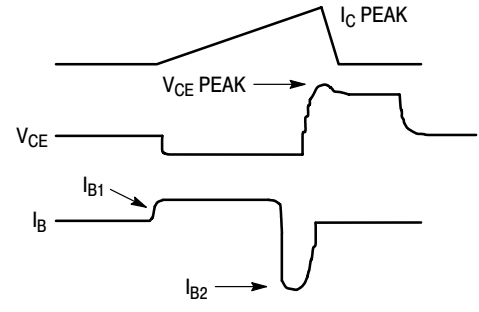
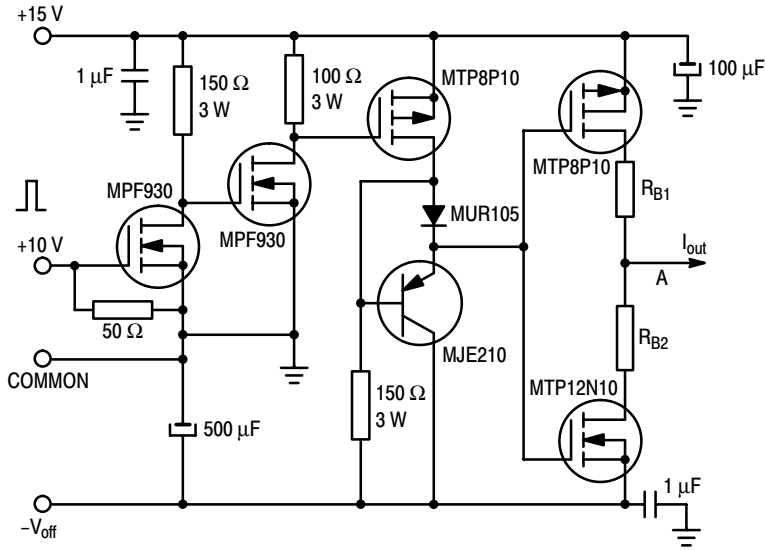


Figure 26. Inductive Switching Measurements

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## TYPICAL SWITCHING CHARACTERISTICS

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$   
 $L = 10 \text{ mH}$   
 $R_{B2} = \infty$   
 $V_{CC} = 20 \text{ Volts}$   
 $I_{C(pk)} = 100 \text{ mA}$

**Inductive Switching**  
 $L = 200 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

**RBSOA**  
 $L = 500 \mu\text{H}$   
 $R_{B2} = 0$   
 $V_{CC} = 15 \text{ Volts}$   
 $R_{B1}$  selected for desired  $I_{B1}$

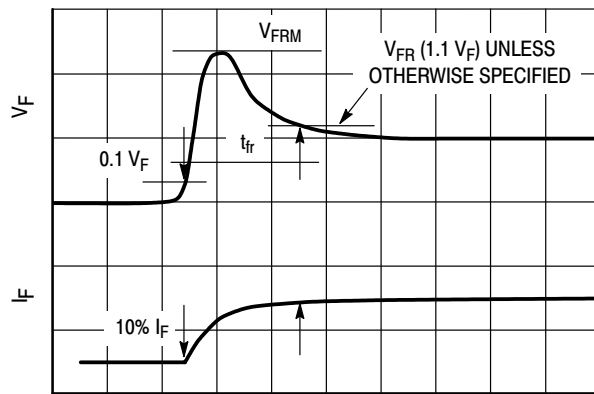


Figure 27.  $t_{fr}$  Measurement

### MAXIMUM RATINGS

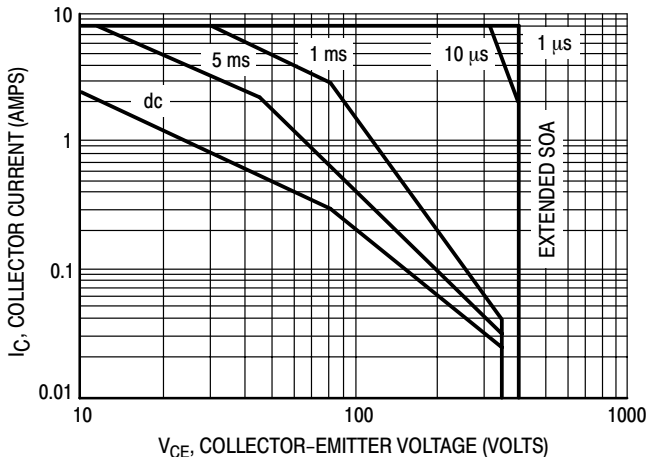


Figure 28. Forward Bias Safe Operating Area

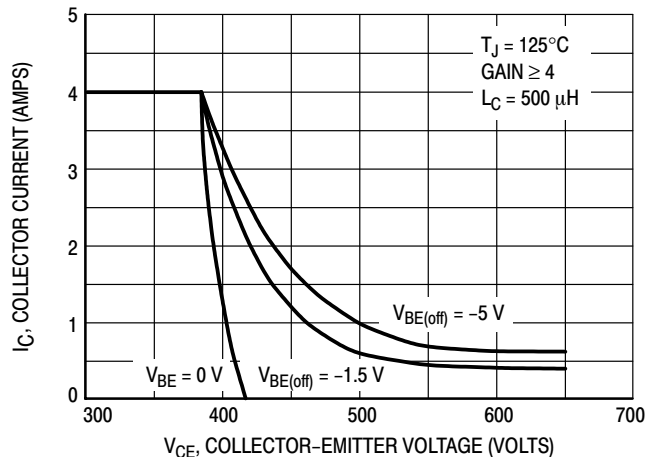
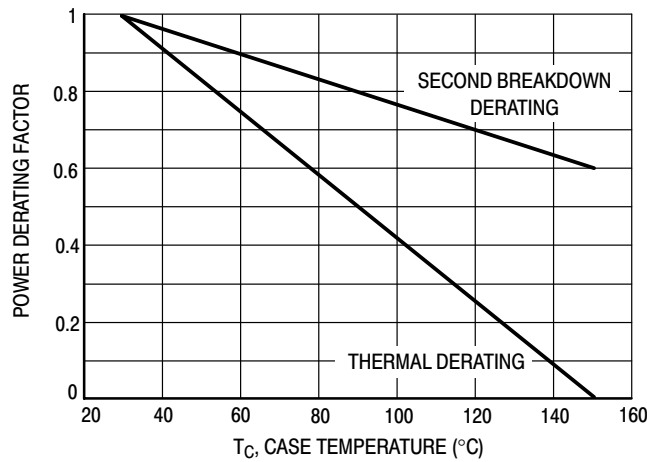


Figure 29. Reverse Bias Safe Operating Area



# BUD42D

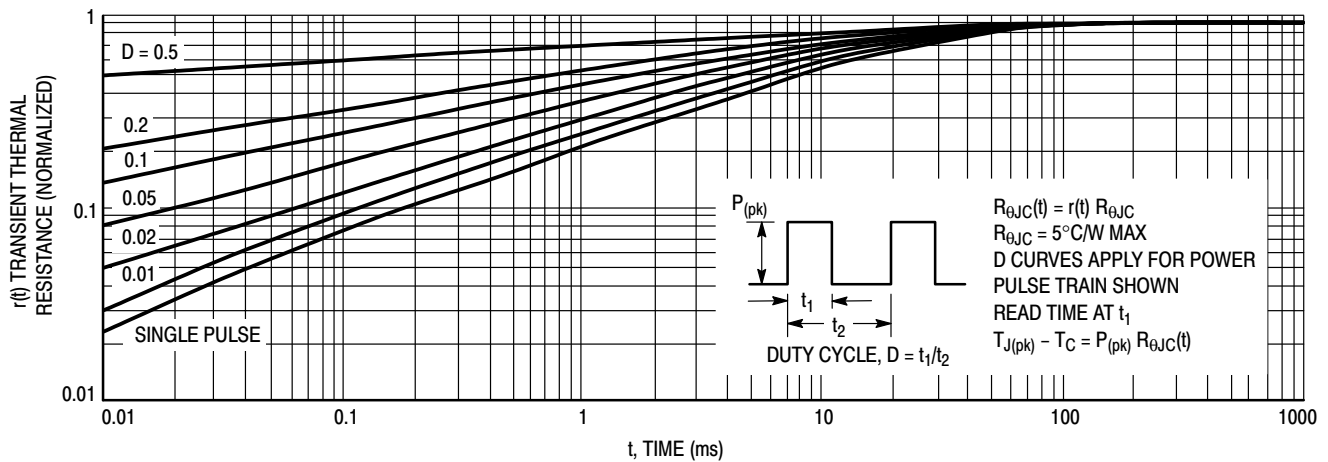


**Figure 30. Power Derating**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 28 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{j(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C > 25^\circ\text{C}$ . Second Breakdown limitations do not derate like thermal limitations. Allowable current at the voltages shown on

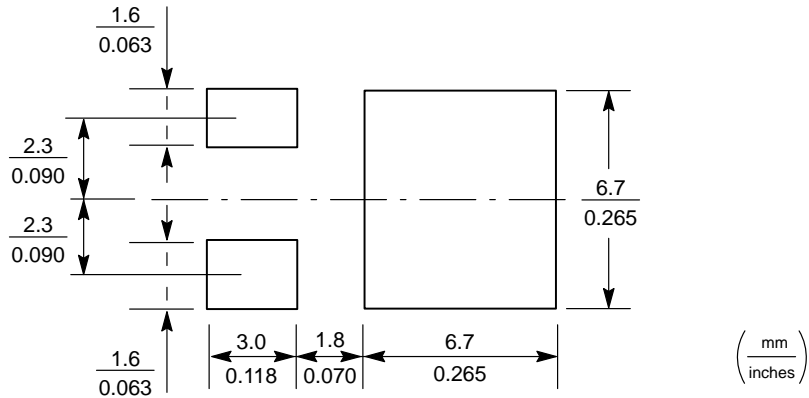
Figure 28 may be found at any case temperature by using the appropriate curve on Figure 30.

$T_{j(pk)}$  may be calculated from the data in Figure 31. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as reverse biased safe operating area (Figure 29). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.



**Figure 31. Thermal Response**

Minimum Pad Sizes Recommended for Surface Mounted Applications



TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 32 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

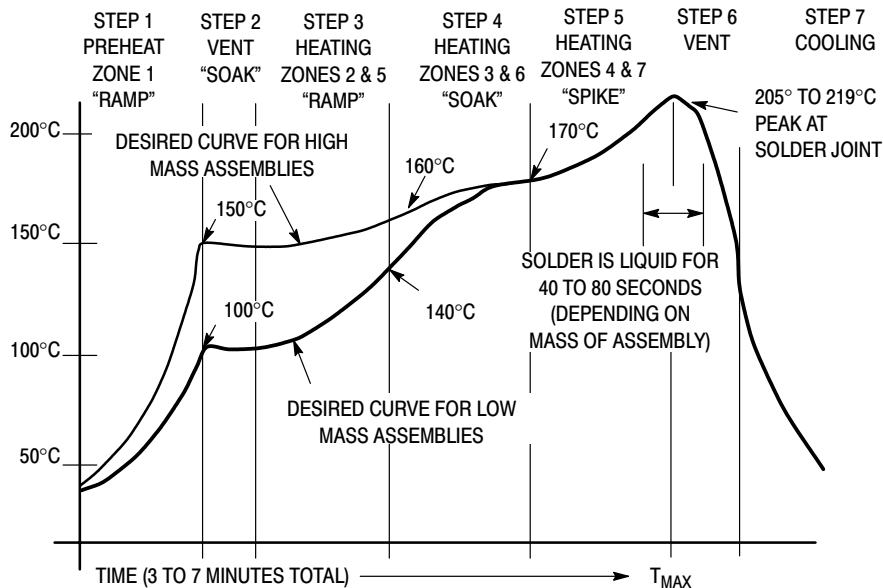
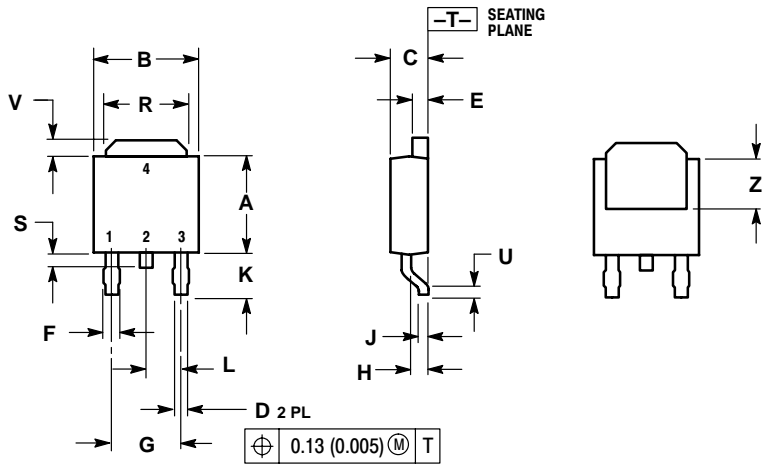


Figure 32. Typical Solder Heating Profile

# BUD42D

## PACKAGE DIMENSIONS

### DPAK CASE 369A-13 ISSUE AB

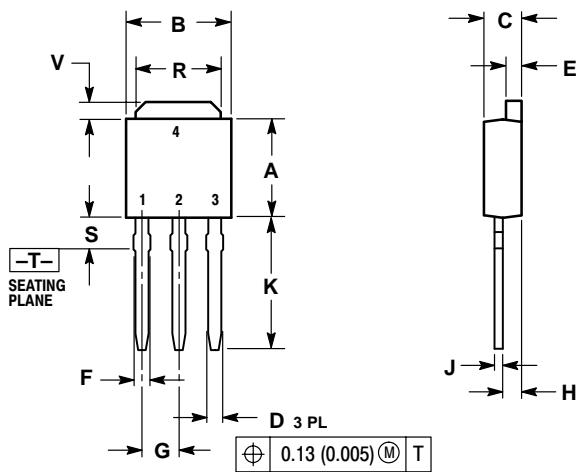


- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

- STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

### DPAK STRAIGHT LEADS CASE 369-07 ISSUE M




- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

- STYLE 1:  
 PIN 1. BASE  
 2. COLLECTOR  
 3. EMITTER  
 4. COLLECTOR

# BUD42D

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