

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HD74HC74

## Dual D-type Flip-Flops (with Preset and Clear)



ADE-205-421 (Z)  
1st. Edition  
Sep. 2000




### Description

The flip-flop has independent data, preset, clear, and clock inputs and Q and  $\bar{Q}$  outputs. The logic level present at the data input is transferred to the output during the positive going transition to the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

### Features

- High Speed Operation:  $t_{pd}$  (Clock to Q or  $\bar{Q}$ ) = 14 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 2  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

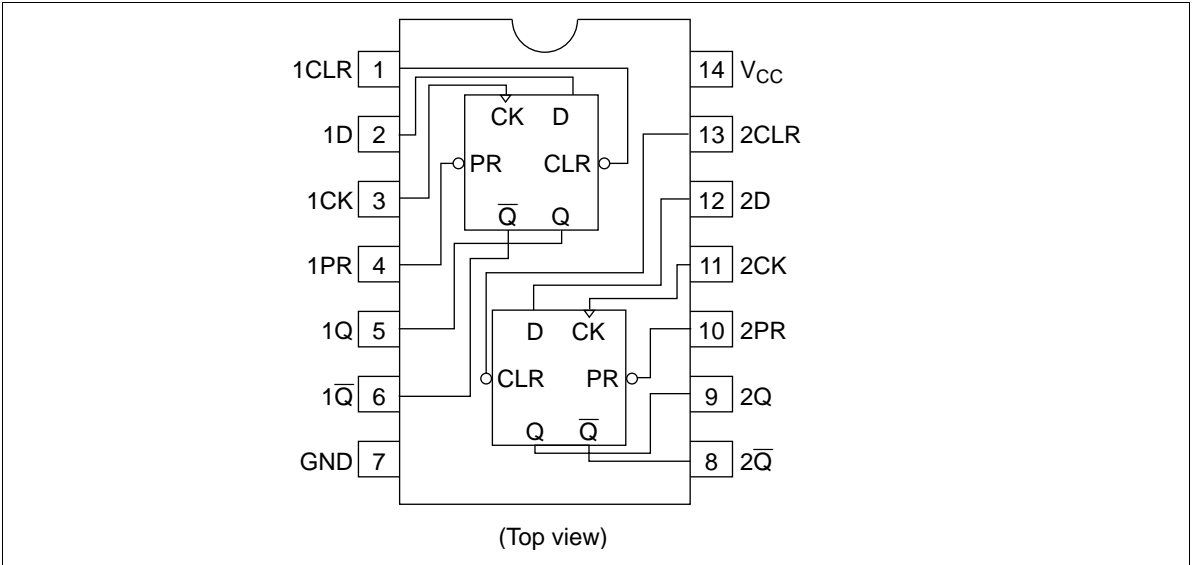
### Function Table

Inputs				Outputs	
Preset	Clear	Clock	Data	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*1	H*1
H	H		H	H	L
H	H		L	L	H
H	H	L	X	no change	no change
H	H	H	X	no change	no change
H	H		X	no change	no change

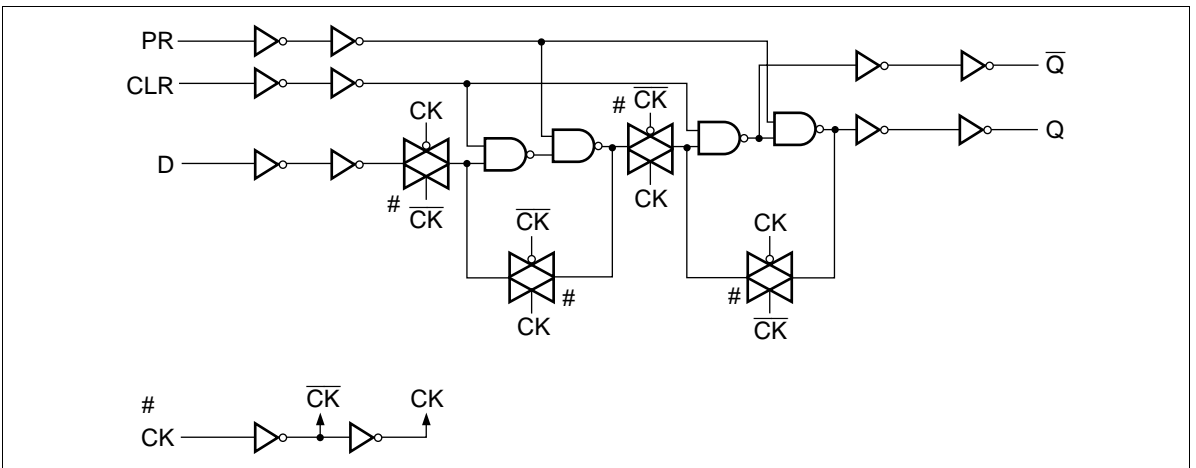
Note: 1. Q and  $\bar{Q}$  will remain HIGH as long as Preset and Clear are Low, but Q and  $\bar{Q}$  are unpredictable, if Preset and Clear go HIGH simultaneously.

# HD74HC74

## Pin Arrangement



## Logic Diagram (1/2)



DC Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min			Max	
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—			I <sub>OH</sub> = -5.2 mA
		V <sub>OL</sub>	2.0	—	0.0	0.1	—			0.1
	4.5		—	0.0	0.1	—	0.1			
	6.0		—	0.0	0.1	—	0.1			
	4.5		—	—	0.26	—	0.33	I <sub>OL</sub> = 4 mA		
	6.0	—	—	0.26	—	0.33	I <sub>OL</sub> = 5.2 mA			
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	2.0	—	20	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA	

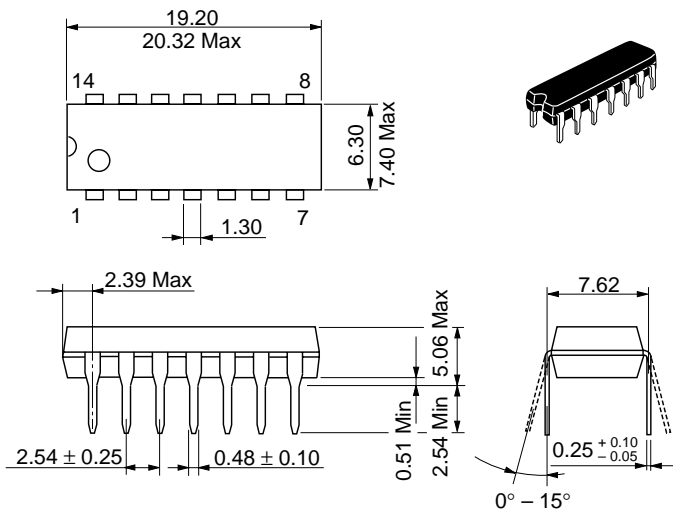
# HD74HC74

## AC Characteristics ( $C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$		$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Maximum clock frequency	$f_{max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	35	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	$t_{PLH}$	2.0	—	—	160	—	200	ns	Clock to Q or $\bar{Q}$
		4.5	—	14	32	—	40		
	$t_{PHL}$	2.0	—	—	27	—	34	ns	Preset or Clear to Q or $\bar{Q}$
		4.5	—	13	32	—	40		
	$t_{su}$	2.0	—	—	27	—	34	ns	Data to Clock
		4.5	20	1	—	25	—		
Setup time	$t_h$	2.0	100	—	—	125	—	ns	Clock to Data
		4.5	20	1	—	25	—		
Hold time	$t_{rem}$	2.0	5	—	—	5	—	ns	Preset, Clear to Clock
		4.5	5	0	—	5	—		
Removal time	$t_w$	2.0	25	—	—	31	—	ns	Clock, Preset, Clear
		4.5	5	-5	—	6	—		
Pulse width	$t_{TLH}$	2.0	80	—	—	100	—	ns	Clock, Preset, Clear
		4.5	16	8	—	20	—		
Output rise/fall time	$t_{THL}$	2.0	—	—	75	—	95	ns	Input Capacitance
		4.5	—	5	15	—	19		
Input Capacitance	$C_{in}$	2.0	—	—	13	—	16	pF	
		4.5	—	—	5	10	—		
		6.0	—	—	5	10	—		

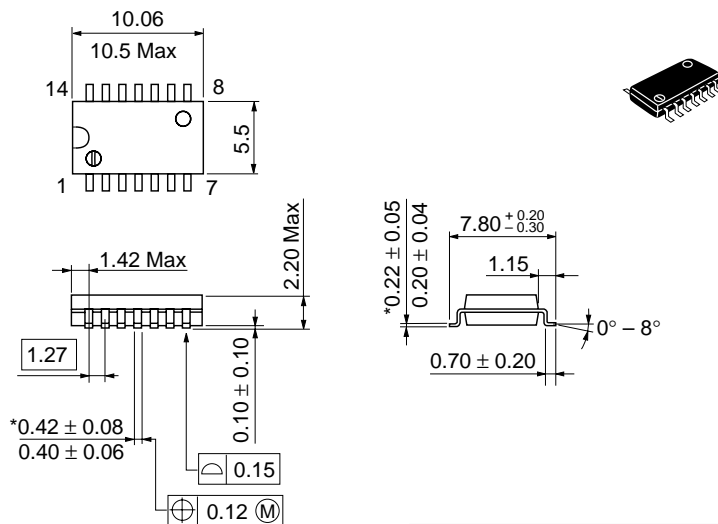
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

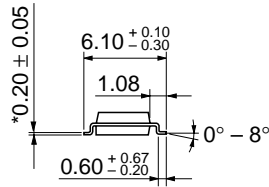
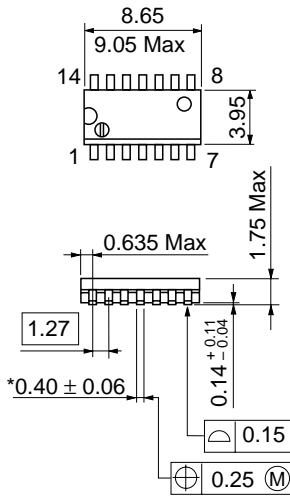
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

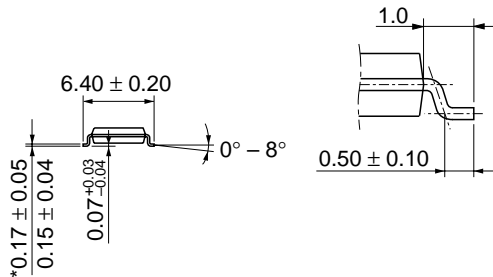
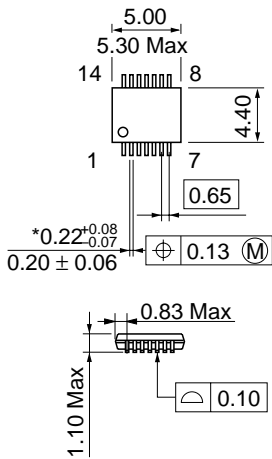
Unit: mm



\*Pd plating

Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g



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