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Octal D-type Transparent Latches (with 3-state outputs)/
Octal D-type Transparent Latches (with inverted 3-state outputs)



ADE-205-555 (Z) 1st. Edition Sep. 2000

### **Description**

When the latch enable input is high, the Q outputs of HD74HCT373 will follow the D inputs and the Q outputs of HD74HCT533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals present at the other inputs and the state of the storage elements.

#### **Features**

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation:  $t_{pd}$  (Data to Q) = 14 ns typ ( $C_L = 50 \text{ pF}$ )
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 4.5$  to 5.5 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max (Ta = 25°C)

#### **Function Table**

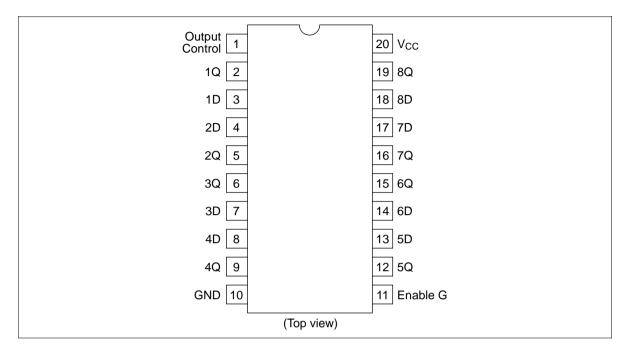
Output Control	Enable G	D	HD74HCT373 Q	HD74HCT533
L	Н	Н	Н	L
L	Н	L	L	Н
L	L	Х	No change	No change
Н	Х	X	Z	Z

X: Irrelevant

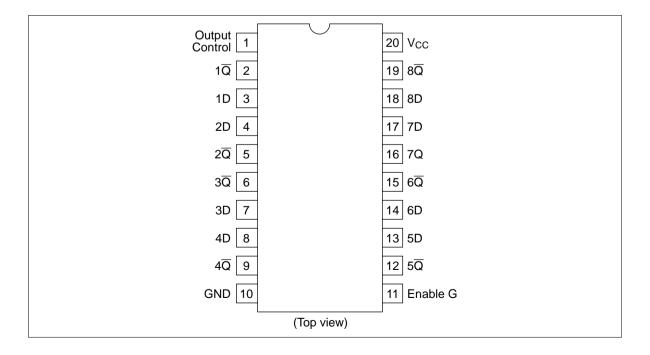
Z: Off (high-impedance) state of a 3-state output.

### **Pin Arrangement**

#### **HD74HCT373**

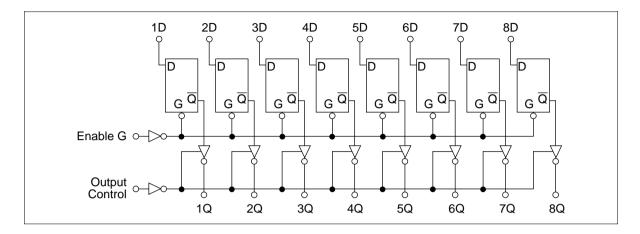


#### **HD74HCT533**

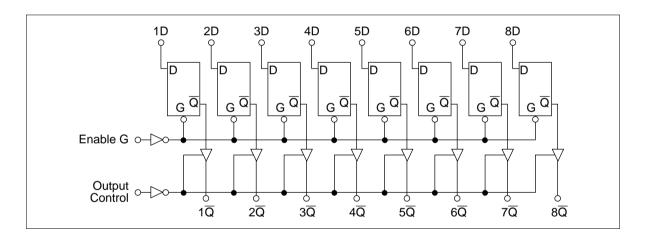


## **Block Diagram**

#### **HD74HCT373**



#### **HD74HCT533**



# **Absolute Maximum Ratings**

Item	Symbol	Rating	Unit
Supply voltage range	V <sub>cc</sub>	-0.5 to +7.0	V
Input voltage	$V_{IN}$	$-0.5$ to $V_{\rm CC}$ + 0.5	V
Output voltage	$V_{\text{out}}$	$-0.5$ to $V_{\rm cc}$ + 0.5	V
DC current drain per pin	I <sub>OUT</sub>	±35	mA
DC current drain per V <sub>CC</sub> , GND	$I_{\rm CC},I_{\rm GND}$	±75	mA
DC input diode current	I <sub>IK</sub>	±20	mA
DC output diode current	I <sub>OK</sub>	±20	mA
Power dissipation per package	P <sub>T</sub>	500	mW
Storage temperature	Tstg	-65 to +150	°C

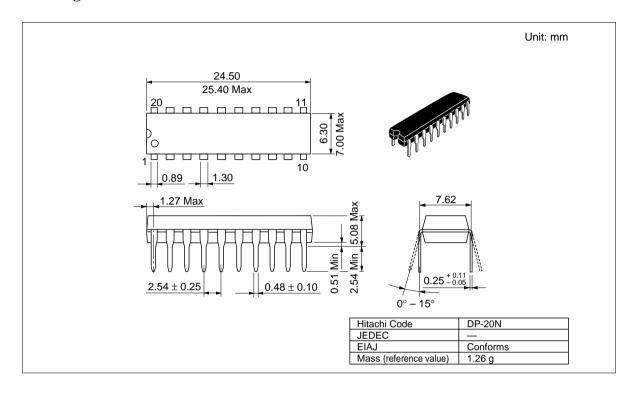
# **DC** Characteristics

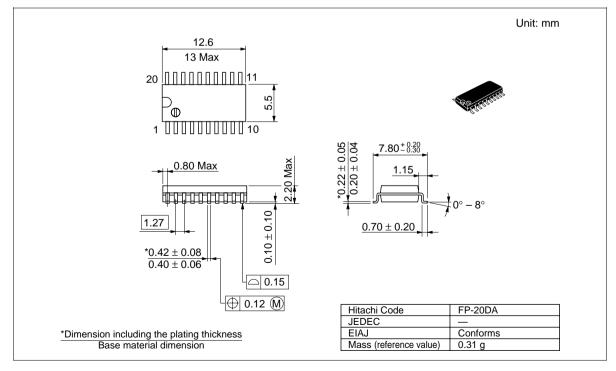
		Ta =	= 25°C	;	Ta = - +85°0	-40 to		Test Co	onditions	
Item	Symbol	Min	Тур	Max	Min	Max	Unit	V <sub>cc</sub> (V)	-	
Input voltage	V <sub>IH</sub>	2.0	_	_	2.0	_	V	4.5 to 5.5		
	V <sub>IL</sub>	_	_	8.0	_	8.0	V	4.5 to 5.5		
Output voltage	V <sub>OH</sub>	4.4	_	_	4.4	_	V	4.5	Vin = V <sub>IH</sub> or V <sub>IL</sub>	$I_{OH} = -20 \mu A$
		4.18	· —	_	4.13	_		4.5	_	$I_{OH} = -6 \text{ mA}$
	$V_{OL}$	_	_	0.1	_	0.1	V	4.5	$Vin = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20 \mu A$
		_	_	0.26	_	0.33		4.5		$I_{OL} = 6 \text{ mA}$
Off-state output current	I <sub>oz</sub>	_	_	±0.5	_	±5.0	μΑ	5.5	$Vin = V_{IH} \text{ or } V_{IL},$ $Vout = V_{CC} \text{ or } C$	
Input current	lin	_	_	±0.1	_	±1.0	μΑ	5.5	Vin = V <sub>CC</sub> or GN	ND
Quiescent current	I <sub>cc</sub>	_	_	4.0	_	40	μΑ	5.5	Vin = V <sub>CC</sub> or GN	ND, lout = 0 μA

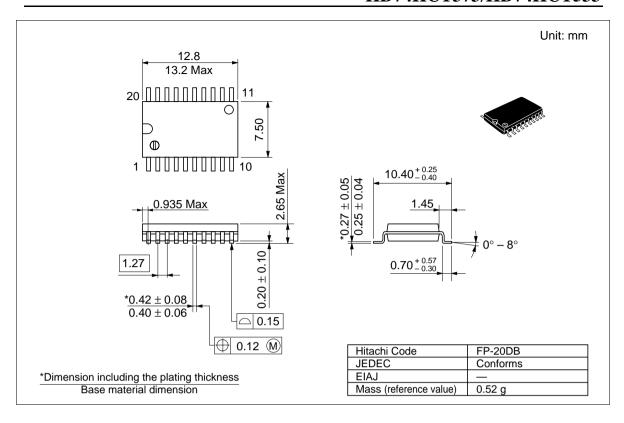
**AC Characteristics** ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

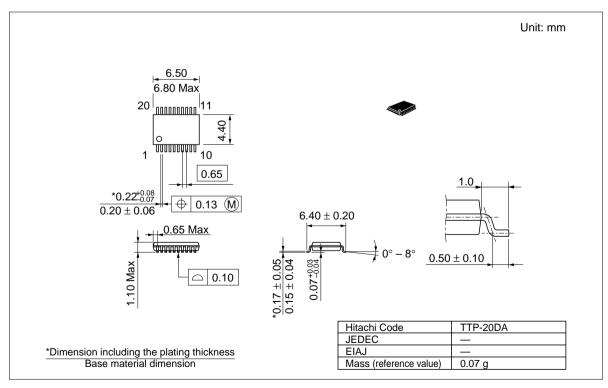
					1a = -	-40 to			
		$Ta = 25^{\circ}C + 85^{\circ}C$			Test Conditions				
Item	Symbol	Min	Тур	Max	Min	Max	Unit	V <sub>cc</sub> (V)	•
Propagation delay	t <sub>PLH</sub>	_	13	30	_	38	ns	4.5	Latch control to Q
time	t <sub>PHL</sub>	_	16	30	_	38		4.5	
	t <sub>PLH</sub>	_	14	25	_	31	ns	4.5	Data to Q
	t <sub>PHL</sub>	_	12	25	_	31	=	4.5	-
Output enable	t <sub>zL</sub>	_	16	30	_	38	ns	4.5	
time	t <sub>zH</sub>	_	15	30	_	38	=	4.5	-
Output disable	t <sub>LZ</sub>	_	14	30	_	38	ns	4.5	
time	t <sub>HZ</sub>	_	16	30	_	38	_	4.5	-
Setup time	t <sub>su</sub>	20	_	_	25	_	ns	4.5	Data to latch control
Hold time	t <sub>h</sub>	10	_	_	13	_	ns	4.5	Latch control to data
Pulse width	t <sub>w</sub>	16	_	_	20	_	ns	4.5	Latch control, output control
Output rise/fall	t <sub>TLH</sub>	_	4	12	_	15	ns	4.5	
time	$t_{THL}$								
Input capacitance	Cin	_	5	10	_	10	pF	_	

## **Package Dimensions**









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