CMOS 4-BIT MICROCONTROLLER

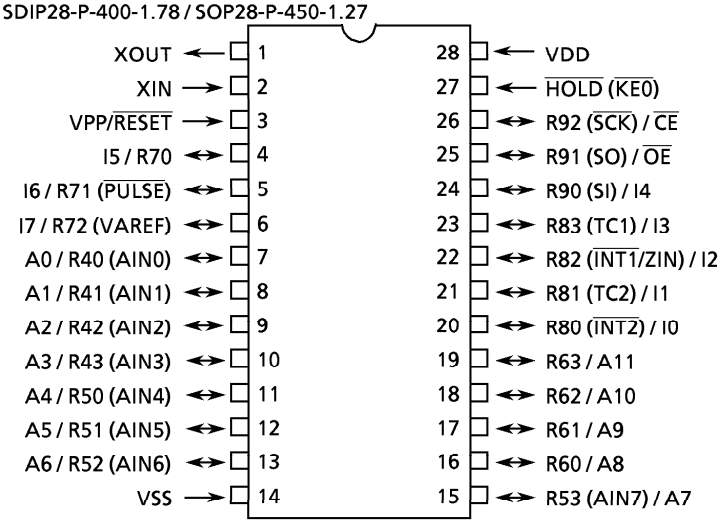
TMP47P443VN
TMP47P443VM
TMP47P443VDM

The 47P443V is the system evaluation LSI of 47C243/443 with 32K bits one-time PROM. The 47P443V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM27256AD.
In addition, the 47P443V and the 47C243/443 are pin compatible. The 47P443V operates as the same as the 47C243/443 by programming to the internal PROM.

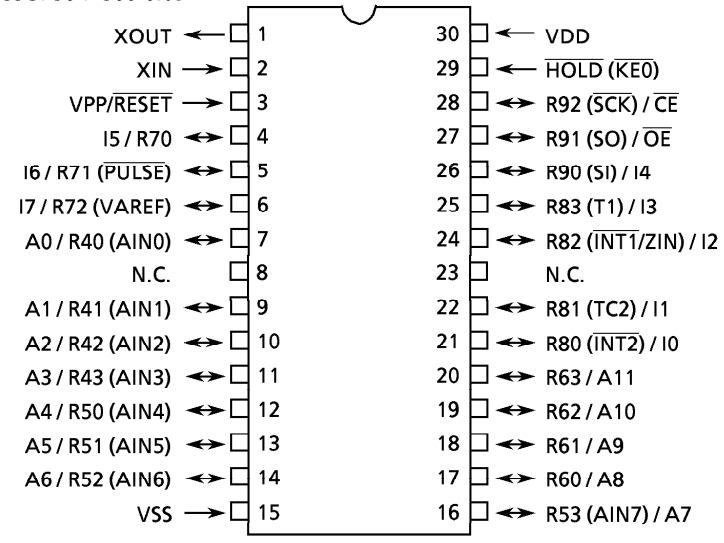
PART No.	ROM	RAM	RACKAGE	ADAPTER SOCKET
TMP47P443VN	OTP 4096 × 8-bit	256 × 4-bit	SDIP28-P-400-1.78	BM11100
TMP47P443VM			SOP28-P-450-1.27	BM11101
TMP47P443VDM			SSOP30-P-300-0.65	BM11115

PIN ASSIGNMENT (TOP VIEW)

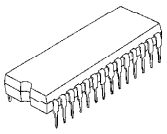
SDIP28-P-400-1.78 / SOP28-P-450-1.27



SSOP30-P-300-0.65

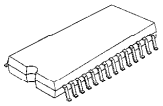


SDIP28-P-400-1.78



TMP47P443VN

SOP28-P-450-1.27



TMP47P443VM

SSOP30-P-300-0.65

TMP47P443VDM

PIN FUNCTION

The 47P443V has MCU mode and PROM mode.

(1) MCU mode

The 47C243/443 and the 47P443V are pin compatible.

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A11 to A8	INPUT	Address inputs	R63 to R60
A7 to A4			R53 to R50
A3 to A0			R43 to R40
I7 to I5	I/O	Data inputs / outputs	R72 to R70
I4			R90
I3 to I0			R83 to R80
$\overline{CE}$	Input	Chip Enable input	R92
$\overline{OE}$		Output Enable input	R91
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	$\overline{RESET}$
VCC		+ 5V	VDD
VSS		0V	VSS
$\overline{HOLD}$	Input	PROM mode setting pin. Be fixed to low level.	
XIN	Input	Input the clock from the external oscillator. (6 MHz typ.)	
XOUT	Input	Be pulled down to VSS level. (750 Ω typ.)	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P443V. The 47P443V is the same as the 47C243/443 except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

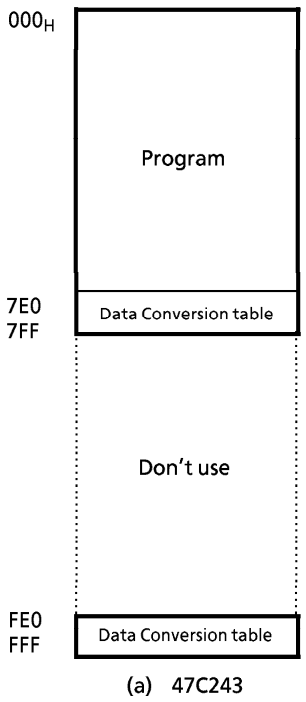
The 47P443V has a MCU mode and a PROM mode.

1.1 MCU mode

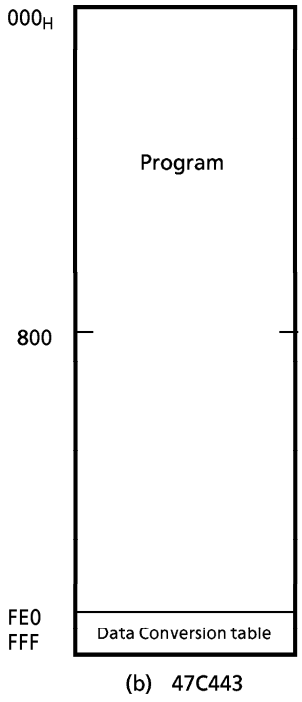
The MCU mode is set by attaching a resonator between the XIN and Xout pins. Operation in the MCU mode is the same as for the 47C243/443. In the 47P443V, RC oscillation is impossible.

1.1.1 Program Memory

The program storage area is the same as for the 47C443. Data conversion tables must be set in two locations when using the 47P443V to check 47C243 operation.

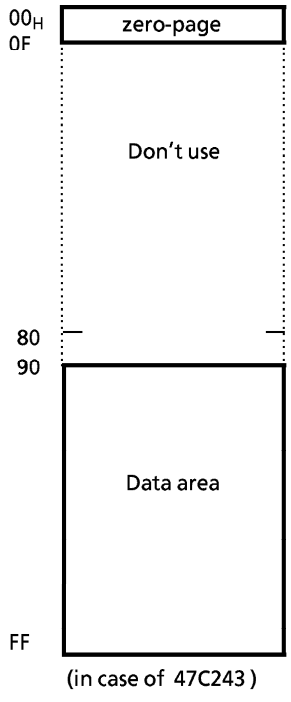


(a) 47C243



(b) 47C443

Figure 1-1. Program area (ROM)



(in case of 47C243)

Figure 1-2. RAM addressing

1.1.2 Data Memory

The 47P443V has 256 × 4-bit of data memory (RAM). When the 47P443V is used as the 47C243 evaluator, programming should be performed assuming that the RAM is assigned to address 00 to $0F_H$ and 90 to FF_H as show in Figure 1-2. When the BM47C443 (emulator) is used as the 47C243 evaluator, it is same.

1.1.3 Input/Output Circuitry

(1) Control pins
47P443V is the same as code SA or SG. In the 47P443V, RC oscillation is impossible. Connecting the resonator is required when using as evaluator of I/O code SD.

(2) I/O Ports
The input/output circuit except pin R72 of the 47P443V is the same as the 47C243/443. In the 47P443V, port option (code SA, SD or SG) of pin R72 is programably selectable.
R72 or VAREF is selected by command register (bit3 of the OP0E). That should be executed over head part on the program. This bit data become dummy data at the 47C243/443. An undefined value is read from bit 2 of the IP07 with an input instruction when VAREF is selecting as the A/D converter analog reference voltage.

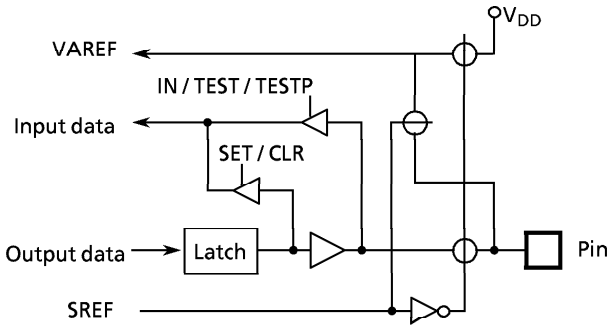


Figure 1-3. R72 (VAREF)

R72/VAREF selector
(Port address : OP0E Initial value : 0000)

3	2	1	0
SREF	0	0	0

SREF	reference voltage selection
0 :	Internal VDD
1 :	External level (VAREF)

Note. Bit 2 to 0 must be set to "0".

Figure 1-4. Command register

1.2 PROM mode

The PROM mode is set by inputting the external clock to the XIN pin when XOUT pin is pulled down to the VSS level. In PROM mode, programs can be written or verified using a general-purpose PROM writer with an adapter socket being attached.

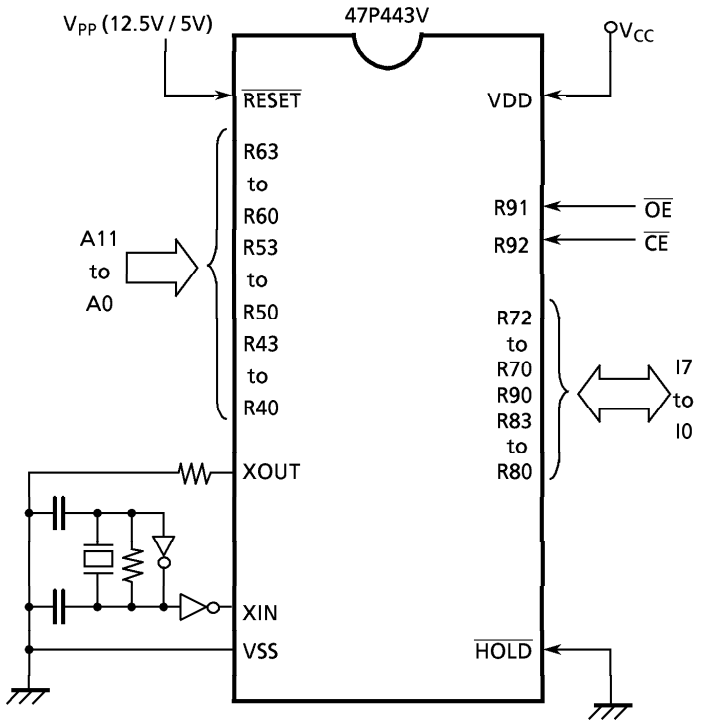


Figure 1-5. Setting for PROM mode

1.2.1 Program Writing

When writing a program, set a ROM type to "57256A" (programming voltage : 12.5V) . Since the 47P443V has a 4096 × 8-bit internal PROM (000 to FFF_H) , set a stop address of a PROM writer to "FFF_H" . For a general-purpose PROM writer, use the writer which does not have or can release an electric signature mode.

Note. When the data written to OTP is same as the data of PROM programmer, there is the possibility that the security writing can not be executed, which is depended on the types of PROM programmers.
In this case, set the data of PROM programmer to "00" and execute the security writing after writing the data to OTP.

1.2.2 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V and $\overline{CE}$ = V_{IH}.

The programming is achieved by applying a single low level 1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC} = V_{PP} = 5V.

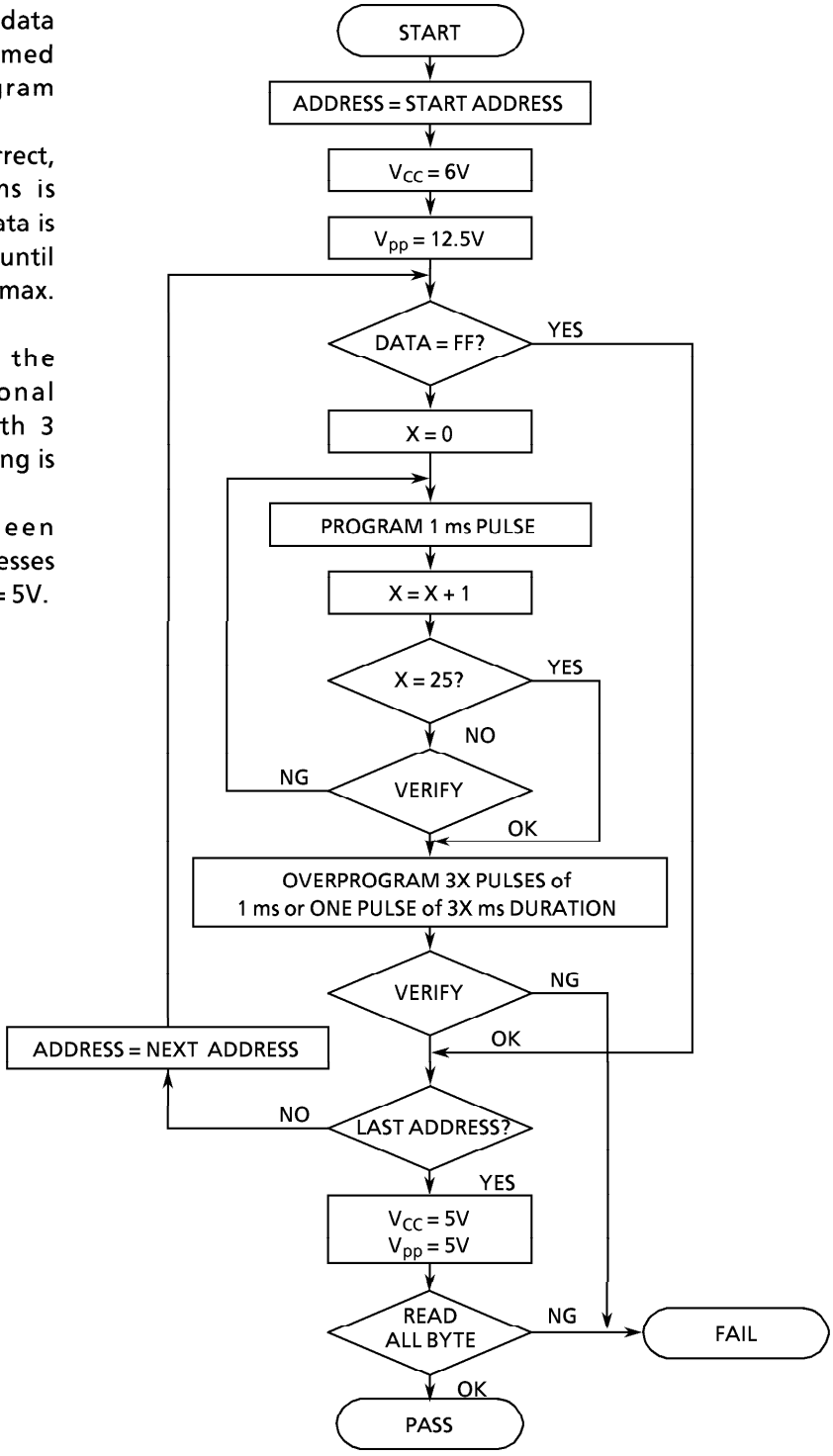


Figure 1-6. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS		RATING	UNIT
Supply Voltage	V_{DD}			– 0.3 to 6.5	V
Program Voltage	V_{PP}	$\overline{RESET}$ / VPP pin		– 0.3 to 13.0	V
Input Voltage	V_{IN}			– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}			– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Port R5, R6		30	mA
	I_{OUT2}	Port R4, R7, R8, R9		3.2	
Output Current (Total)	ΣI_{OUT1}	Port R4, R5, R6, R7, R8, R9		120	mA
Power Dissipation [T_{opr} = 70 °C]	PD		DIP	300	mW
			SOP	180	
			SSOP	145	
Soldering Temperature (time)	T_{sld}			260 (10 s)	°C
Storage Temperature	T_{stg}			– 55 to 125	°C
Operating Temperature	T_{opr}			– 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 8.0MHz	2.7	5.5	V
			fc = 4.2MHz	2.2		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	In the normal operating area	V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		V_{DD} × 0.75		
	V_{IH3}		In the HOLD mode	V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	In the normal operating area	0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.25	
	V_{IL3}		In the HOLD mode		V_{DD} × 0.1	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5V	0.4	8.0	MHz
			V_{DD} = 2.2 to 5.5V		4.2	

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	$\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.5V, V_{OUT} = 5.5V	–	–	2	μA
Output Low Voltage	V_{OL}	Port R4, R7, R8, R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
			V_{DD} = 2.2V, I_{OL} = 20μA	–	–	0.1	
Output Low Current	I_{OL1}	Port R5, R6	V_{DD} = 4.5V, V_{OL} = 1.0V	7	20	–	mA
Supply Current (in the Normal operating mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	–	2	4	mA
			V_{DD} = 3.0V, fc = 4MHz	–	1	2	
			V_{DD} = 3.0V, fc = 400kHz	–	0.5	1	
Supply Current (in the HOLD operating mode)	I_{DDH}		V_{DD} = 5.5V	–	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, V_{DD} = 5V.
Note 2. Input Current I_{IN1} : The current through resistor is not included.
Note 3. Supply Current : The analog supply current (I_{REF}) is not included.
Note 4. Supply Current : V_{IN} = 5.3V / 0.2V (V_{DD} = 5.5V), 2.8V / 0.2V (V_{DD} = 3.0V)

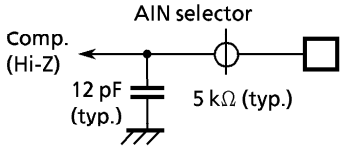
A / D CONVERSION CHARACTERISTICS (T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{SS}	2.7	—	—	V
Analog Input Voltage	V_{AIN}		V_{SS}	—	V_{DD}	V
Analog Supply current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 2.7 to 5.5V, V_{AREF} = V_{DD} ± 0.001V, V_{SS} = ± 0.001V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

A.C. CHARACTERISTICS (V_{SS} = 0V, Topr = – 30 to 70 °C)

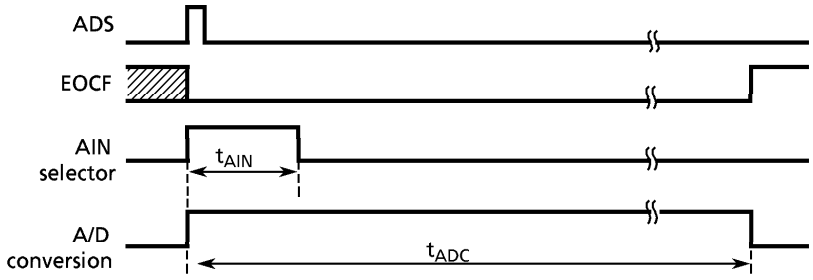
PARAMETER	SYMBOL	CONDITIONS		Min.	Typ.	Max.	UNIT
Instruction Cycle Time	tcy		V_{DD} = 2.7 to 5.5V	1.0	–	20	μs
			V_{DD} = 2.2 to 5.5V	1.9			
High level clock pulse width	t_{WCH}	For external clock (XIN input)	$V_{DD} \geqq 2.7V$	80	–	–	ns
			$V_{DD} < 2.7V$	120			
Low level clock pulse width	t_{WCL}		$V_{DD} \geqq 2.7V$	80			
			$V_{DD} < 2.7V$	120			
A/D Conversion Time	t_{ADC}			–	24 tcy	–	μs
A/D Sampling Time	t_{AIN}			–	2 tcy	–	
Shift data Hold Time	t_{SDH}			0.5 tcy – 300	–	–	ns

Note 1 A/D conversion timing :
Internal circuit for pins AIN0 to 7

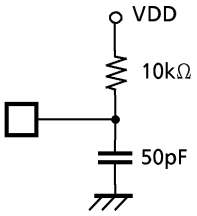


* Electrical change inust be loaded into the buit-in condensen during t_{AIN} for normal A/D conversion.

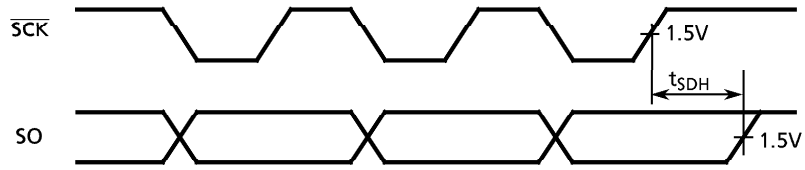
A/D conversion timing



Note2 Shift data Hold Time :
External circuit for pins
$\overline{SCK}$ and SO



Serial port (completed of transmission)



ZERO-CROSS DETECTION CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 30 to 70℃)

Characteristics are equivalent to the 47C243/443's.

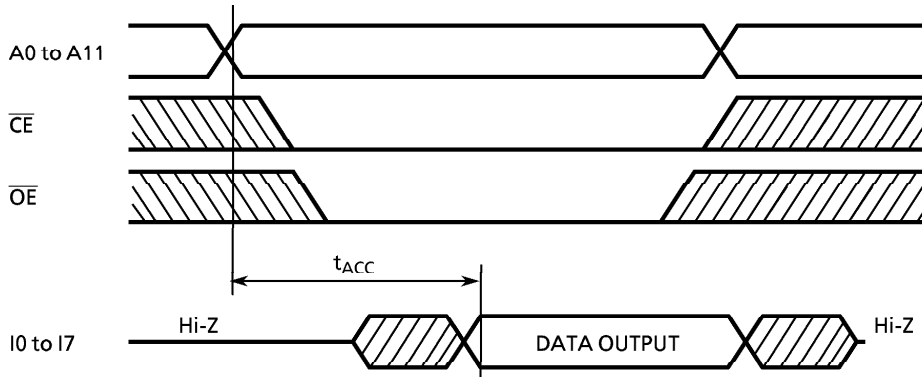
RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 2.2 to 5.5V, T_{opr} = – 30 to 70℃)

Recommended oscillating conditions of the 47P443V are equal to the 47C243/443's but RC oscillation is impossible.

DC/AC CHARACTERISTICS (V_{SS} = 0V)

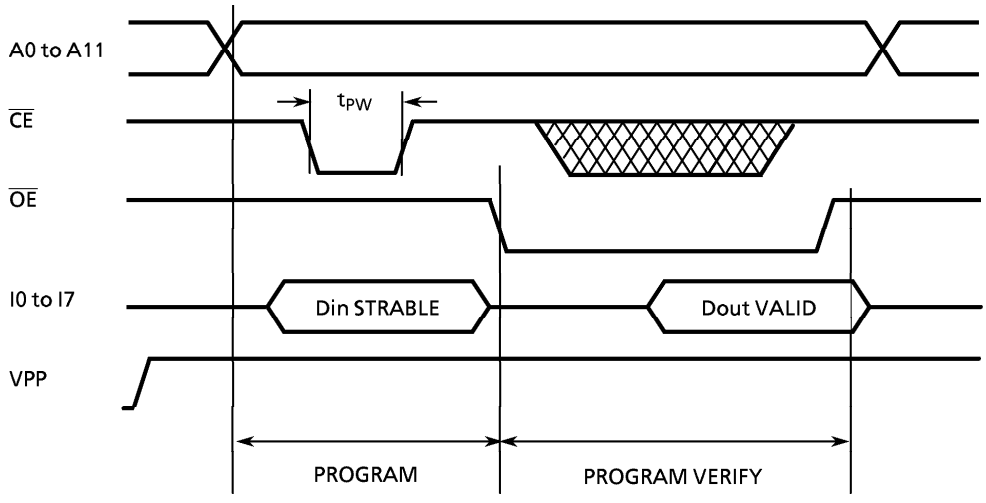
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns

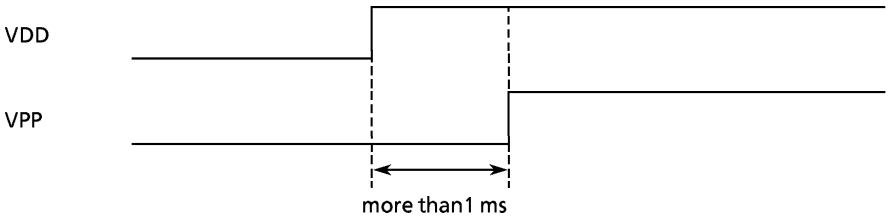


(2) High Speed Programming Operation

PARAMETER	SYBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25V	0.95	1.0	1.05	ms



Note. There are some PROM programmer types which cannot program OTP.
In TMP47P443V, VPP pin is also used as RESET pin. To set a mode, REST/VPP pin must be set to "low" during 1 ms and more after the rising of power-on and the rising of VDD electrical power.



Recommended EPROM programmer

TYPE	
R4945	(ADVANTEST)
UNISITE	(DATA I/O)
AF – 9706	(ANDO)
PECKER – 11	(AVAL DATA)