

# T6C63

## COLUMN DRIVER FOR A DOT MATRIX LCD

The T6C63 is a 240-channel-output column driver for an STN dot matrix LCD.

The T6C63 features a 42-V LCD drive voltage and a 20-MHz maximum operating frequency. The T6C63 is able to drive LCD panels with a duty ratio of up to 1 / 480.

It is recommended for use with the T6C14.

### FEATURES

- Display duty application : to 1 / 480
- LCD drive signal : 240
- Data transfer : 8-bit bidirectional
- Operating frequency : 20 MHz (V<sub>DD</sub> = 4.5 V)  
12.5 MHz (V<sub>DD</sub> = 2.7 V)
- LCD drive voltage : 14 to 42 V (max 45 V)
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : -20 to 75°C
- LCD drive output resistance : 700Ω (typ.), 1200Ω (max) (20 V, 1 / 13 bias)
- Display-off function : When / DSPOF is L, all LCD drive outputs (O1 to O240) remain at the V<sub>5</sub> level.
- Low power consumption : Cascade connection and auto enable transfer functions are available.

Unit: mm		
T6C63	LEAD PITCH	
	IN	OUT
(UAN, 3NS)	0.60	0.074

Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

**TCP (Tape Carrier Package)**

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● Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.

● Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.

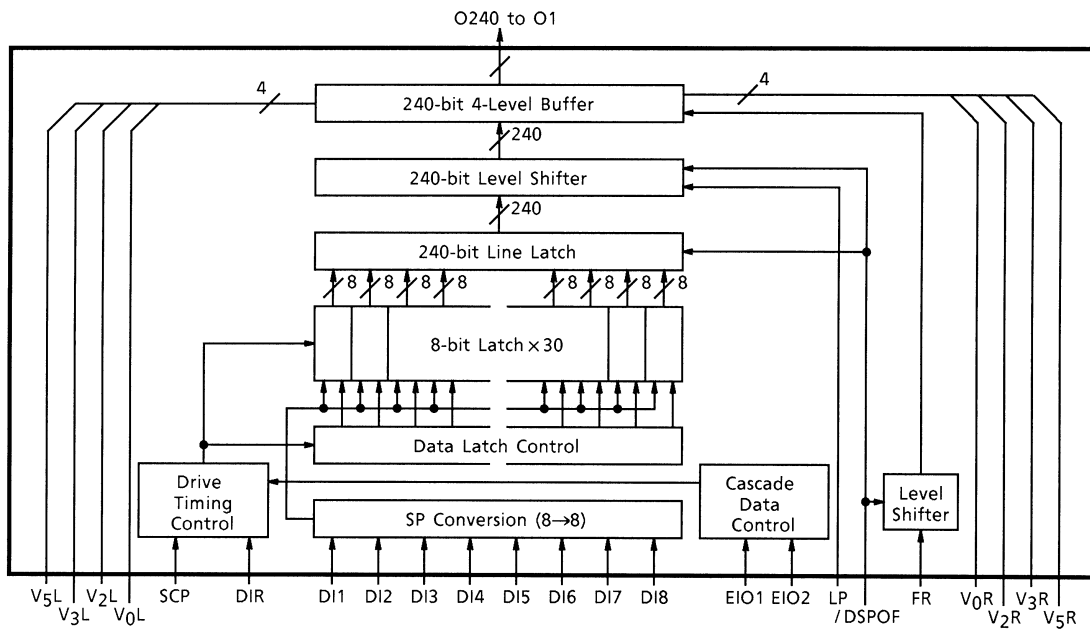
This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.

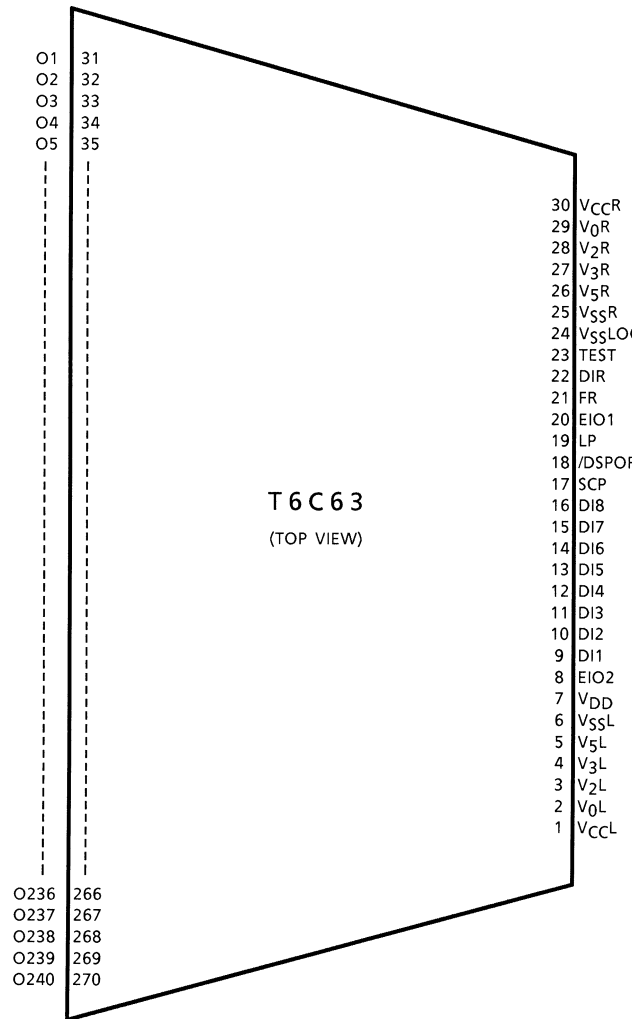
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**BLOCK DIAGRAM**



**PIN ASSIGNMENT**

\* : The above diagram shows the pin configuration of the LSI Chip, not that of the tape carrier package.

## PIN FUNCTIONS

PIN NAME	I / O	FUNCTIONS	LEVEL
O1 to O240	Output	Output for LCD drive signal	$V_0$ to $V_5$
EIO1, EIO2	I / O	Input / output for enable signal DIR selects In or Out. Connect EIO (IN) of 1st LSI to L. For a cascade connection, connect EIO (OUT) to EIO (IN) of next LSI (refer to page 6).	$V_{DD}$ to $V_{SS}$
DI1 to DI8	Input	Input for data signal Input for data signal	
DIR	Input	(Direction) Input for data flow direction select	
/ DSPOF	Input	(Display off) / DSPOF = L: Display-off mode, (O1 to O240) remain at the $V_5$ level / DSPOF = H: Display-on mode, (O1 to O240) are operational.	
LP	Input	(Latch pulse) Display data is latched on falling edges of LP. When EIO (IN) = L, SCP·LP = H enables the 1st LSI.	
FR	Input	(Frame) Input for frame signal	
SCP	Input	(Shift clock pulse) Input for shift clock pulse	
TEST	—	(Test) Fix to L or open	
$V_{DD}$	—	Power supply for internal logic (5.0 V)	
$V_{SS}LOG$	—	Power supply for internal logic (0 V)	
$V_{SS}L\cdot R$	—	Power supply for LCD drive circuit	
$V_5L\cdot R$	—	Power supply for LCD drive circuit	
$V_{3/4}L\cdot R$	—	Power supply for LCD drive circuit	
$V_{2/1}L\cdot R$	—	Power supply for LCD drive circuit	
$V_0L\cdot R$	—	Power supply for LCD drive circuit	
$V_{CCL}\cdot R$	—	Power supply for LCD drive circuit	

## RELATION BETWEEN FR, DATA INPUT AND OUTPUT LEVEL

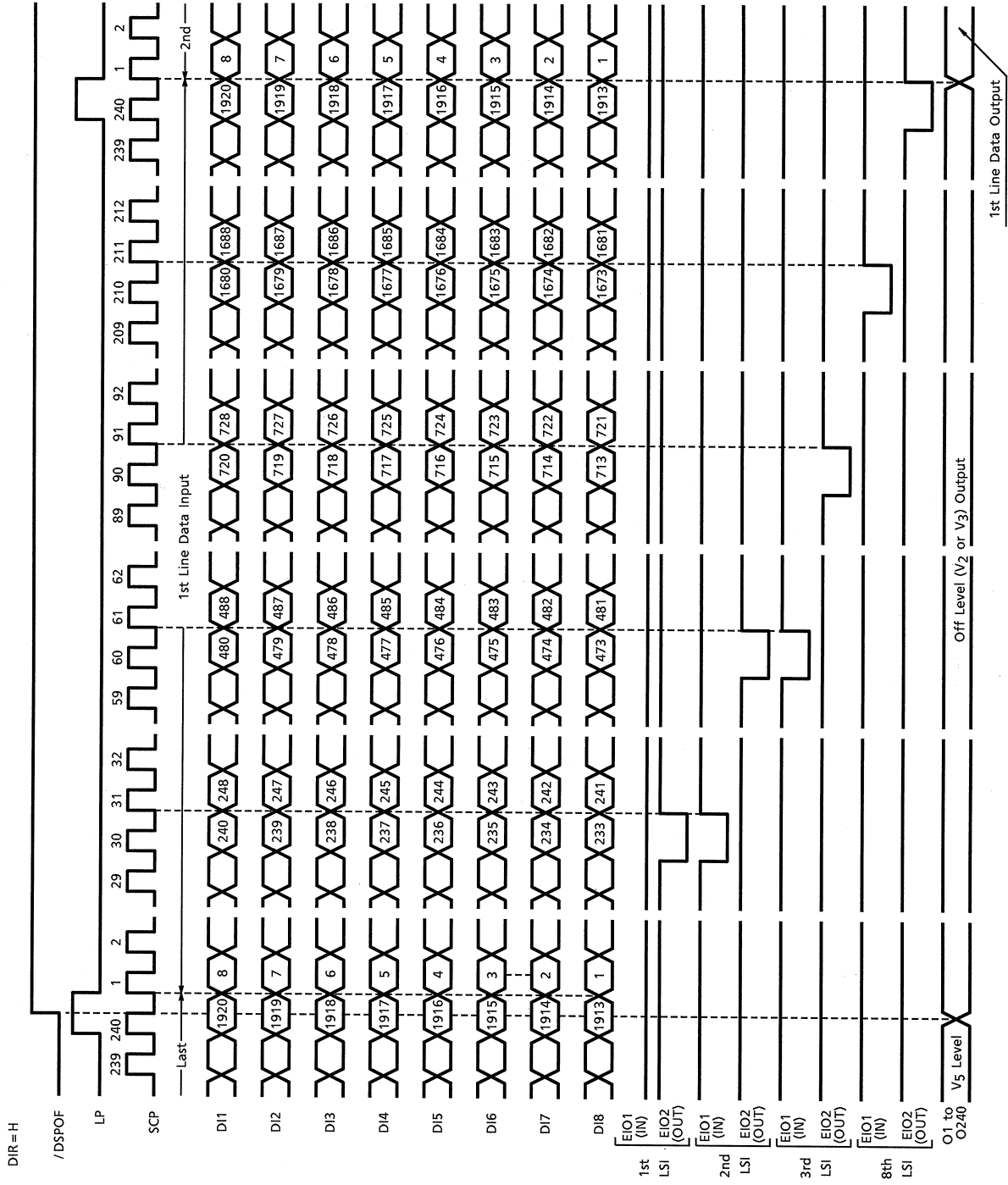
F R	DATA INPUT (DI1 to DI8)	/ DSPOF	OUTPUT LEVEL
H	L	H	V <sub>2</sub>
H	H	H	V <sub>0</sub>
L	L	H	V <sub>3</sub>
L	H	H	V <sub>5</sub>
—	—	L	V <sub>5</sub>

## DATA INPUT FORMAT

DIR	ENABLE PIN		(*1)	INPUT DATA LINE AND OUTPUT BUFFERS							
	(EIO1)	(EIO2)		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	IN	OUT	L	O240	O239	O238	O237	O236	O235	O234	O233
			F	O8	O7	O6	O5	O4	O3	O2	O1
L	OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
			F	O233	O234	O235	O236	O237	O238	O239	O240

\*1 : L: Last Data F: First Data

TIMING DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

(Ensure that the following conditions are maintained:  $V_{CC} \geq V_0 \geq V_2 \geq V_3 \geq V_5 \geq V_{SS}$ )

ITEM	SYMBOL	PIN NAME	RATING	UNIT
Supply Voltage 1	$V_{DD}$	$V_{DD}$	-0.3 to 6.5	V
Supply Voltage 2	$V_{CC}$	$V_{CCL} / R$	-0.3 to 45.0	V
Supply Voltage 3	$V_0, V_2$	$V_0L / R, V_2, 1L / R$	-0.3 to $V_{CC} + 0.3$	V
Supply Voltage 4	$V_3, V_5$	$V_3, 4L / R, V_5L / R$	-0.3 to $V_{CC} + 0.3$	V
Input Voltage	$V_{IN}$	(*2)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	$T_{opr}$	—	-20 to 75	°C
Storage Temperature	$T_{stg}$	—	-40 to 125	°C

\*2 : SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, / DSPOF, TEST

## ELECTRICAL CHARACTERISTICS

### DC CHARACTERISTICS

(Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 2.7$  to  $5.5 V$ ,  $T_a = -20$  to  $75^\circ C$ )

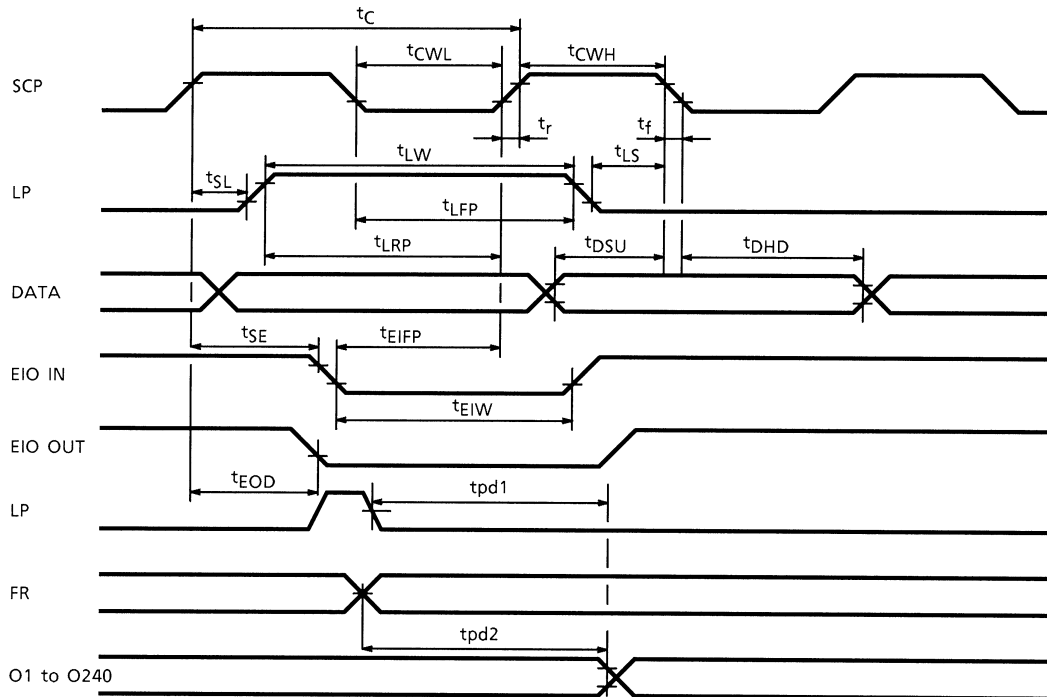
ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITION			MIN	TYP.	MAX	UNIT	PIN NAME
Supply Voltage 1	$V_{DD}$	—	—			2.7	5.0	5.5	V	$V_{DD}$
Supply Voltage 2	$V_{CC}$	—	—			14.0	—	42.0		$V_{CCL} / R$
Input Voltage	H Level	$V_{IH}$	—			0.8 $V_{DD}$	—	$V_{DD}$		SCP, FR, LP, DIR, EIO1, EIO2, DI1 to DI8, / DSPOF, TEST
	L Level	$V_{IL}$	—			0	—	0.2 $V_{DD}$		
Output Voltage	H Level	$V_{OH}$	$I_{OH} = -0.5 \text{ mA}$			$V_{DD} - 0.5$	—	$V_{DD}$	EIO1 EIO2	
	L Level	$V_{OL}$	$I_{OL} = 0.5 \text{ mA}$			0	—	0.5		
Output Resistance	H Level	$R_{OH}$	$V_{OUT} = V_0 - 0.5 \text{ V}$ (*3)			—	700	1200	$\Omega$	O1 to O240
	M Level	$R_{OM}$	$V_{OUT} = V_2 \pm 0.5 \text{ V}$ (*3)			—	700	1200		
		$R_{OM}$	$V_{OUT} = V_3 \pm 0.5 \text{ V}$ (*3)			—	700	1200		
	L Level	$R_{OL}$	$V_{OUT} = V_5 + 0.5 \text{ V}$ (*3)			—	700	1200		
Input Current	$I_{IL}$	—	$V_{DD}$	$V_{CC}$	CONDITION	-10	—	10	$\mu A$	$V_0L / R$ $V_2L / R$ $V_3L / R$ $V_5L / R$
			5.0	42	Standby					
Current Consumption	$I_{DD} \text{ Ope}$	—	5.0	20	Function (*4)	—	—	5.0	mA	$V_{DD}$
			2.7	20		—	—	2.5		
	$I_{DD} \text{ St / by}$	—	5.0	20	Function (*5)	—	—	2.0		
			2.7	20		—	—	1.0		
	$I_{CC} \text{ Leak}$	—	5.0	42	Standby	-10	—	10		

\*3 :  $V_{CC} = 20 V$ , 1 / 13 bias

\*4 :  $f_{scp} = 13 \text{ MHz}$ ,  $f_{LP} = 54 \text{ kHz}$ ,  $f_{FR} = 13.5 \text{ kHz}$ ,  $f_{EIO} = 650 \text{ kHz}$ ,  
Data Format: every bit inverted, while internal data receiver is operating

\*5 :  $f_{scp} = 13 \text{ MHz}$ ,  $f_{LP} = 54 \text{ kHz}$ ,  $f_{FR} = 13.5 \text{ kHz}$ ,  
Data Format: every bit inverted, Internal data receiver is sleeping

## AC ELECTRICAL CHARACTERISTICS



### TEST CONDITIONS (1) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 4.5\text{ to }5.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	$t_C$	—	50	—	—	ns
SCP Pulse Width	$t_{CWL}$ , $t_{CWH}$	—	10	—	—	
Data Set-Up Time	$t_{DSU}$	—	8	—	—	
Data Hold Time	$t_{DHD}$	—	10	—	—	
SCP Rise / Fall Time	$t_r$ , $t_f$	—	—	—	(*6)	
LP Rise Time	$t_{LRP}$	—	11	—	—	
LP Fall Time	$t_{LFP}$	—	7	—	—	
LP Pulse Width	$t_{LW}$	—	7	—	—	
SCP-to-LP Delay Time (SLP → LP)	$t_{SL}$	—	0	—	—	
LP-to-SCP Delay Time (LP → SCP)	$t_{LS}$	—	7	—	—	
EIO IN Rise Time	$t_{EIFP}$	—	20	—	—	
EIO IN Pulse Width	$t_{EIW}$	—	9	—	—	
SCP-to-EIO Delay Time (SCP → EIO)	$t_{SE}$	—	1	—	—	
EIO-OUT Delay Time	$t_{EOD}$	(*7)	—	—	20	
Output Delay Time 1 (LP → OUT)	$t_{pd1}$	—	—	—	400	
Output Delay Time 2 (FR → OUT)	$t_{pd2}$	—	—	—	400	
Output Delay Time Variation	(*8)	—	—	0	30	

\*6 :  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r, t_f \leq 50\text{ ns}$

\*7 :  $C_L = 10\text{ pF}$

\*8 : Variation between output pins in  $t_{pd1}$  and  $t_{pd2}$ .



TEST CONDITIONS (2) ( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 2.7\text{ to }4.5\text{ V}$ ,  $V_{CC} = 14\text{ to }42\text{ V}$ ,  $T_a = -20\text{ to }75^\circ\text{C}$ )

ITEM	SYMBOL	TEST CONDITION	MIN	TYP.	MAX	UNIT
Clock Cycle	$t_C$	—	80	—	—	ns
SCP Pulse Width	$t_{CWH}$ , $t_{CWL}$	—	20	—	—	
Data Set-Up Time	$t_{DSU}$	—	15	—	—	
Data Hold Time	$t_{DHD}$	—	10	—	—	
SCP Rise / Fall Time	$t_r$ , $t_f$	—	—	—	(*9)	
LP Rise Time	$t_{LRP}$	—	15	—	—	
LP Fall Time	$t_{LFP}$	—	14	—	—	
LP Pulse Width	$t_{LW}$	—	14	—	—	
SCP-to-LP Delay Time	$t_{SL}$	—	2	—	—	
LP-to-SCP Delay Time	$t_{LS}$	—	14	—	—	
EIO IN Fall Time	$t_{EIFP}$	—	20	—	—	
EIO IN Pulse Width	$t_{EIW}$	—	14	—	—	
SCP-to-EIO Delay Time	$t_{SE}$	—	2	—	—	
EIO-OUT Delay Time	$t_{EOD}$	(*10)	—	—	36	
Output Delay Time 1 (LP → OUT)	$t_{pd1}$	—	—	—	500	
Output Delay Time 2 (FR → OUT)	$t_{pd2}$	—	—	—	500	
Output Delay Time Variations	(*11)	—	—	0	50	

\*9 :  $t_r$ ,  $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r$ ,  $t_f \leq 50\text{ ns}$

\*10 :  $C_L = 10\text{ pF}$

\*11 : Variation between output pins in  $t_{pd1}$  and  $t_{pd2}$

NOTE: Insert the bypass capacitor (0.1 $\mu\text{F}$ ) between  $V_{DD}$  and  $V_{SS}$ , and between  $V_{CC}$  and  $V_{SS}$  to decrease power supply noise.

Place the bypass capacitor as close to the LSI as possible.