DESCRIPTION

Hynix HYMD1326458-H/L series is unbuffered 184-pin double data rate Synchronous DRAM Dual In-Line Memory Modules (DIMMs) which are organized as 32Mx64 high-speed memory arrays. Hynix HYMD1326458-H/L series consists of sixteen 16Mx8 DDR SDRAM in 400mil TSOP II packages on a 184pin glass-epoxy substrate. Hynix HYMD1326458-H/L series provide a high performance 8-byte interface in 5.25" width form factor of industry standard. It is suitable for easy interchange and addition.

Hynix HYMD1326458-H/L series is designed for high speed of up to 133MHz and offers fully synchronous operations referenced to both rising and falling edges of differential clock inputs. While all addresses and control inputs are latched on the rising edges of the clock, Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2. High speed frequencies, programmable latencies and burst lengths allow variety of device operation in high performance memory system.

Hynix HYMD1326458-H/L series incorporates SPD(serial presence detect). Serial presence detect function is implemented via a serial 2,048-bit EEPROM. The first 128 bytes of serial PD data are programmed by Hynix to identify DIMM type, capacity and other the information of DIMM and the last 128 bytes are available to the customer.

FEATURES

- 256MB (32M x 64) Unbuffered DDR DIMM based on 16Mx8 DDR SDRAM
- JEDEC Standard 184-pin dual in-line memory module (DIMM)
- 2.5V +/- 0.2V VDD and VDDQ Power supply
- All inputs and outputs are compatible with SSTL_2 interface
- Fully differential clock operations (CK & /CK) with 100MHz/125MHz/133MHz
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Data(DQ), Data strobes and Write masks latched on both rising and falling edges of the clock
- Data inputs on DQS centers when write (centered DQ)
- Data strobes synchronized with output data for read and input data for write
- Programmable CAS Latency 2 / 2.5 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- 4096 refresh cycles / 64ms

ORDERING INFORMATION

Part No.	Power Suppy	Clock Frequency	Interface	Form Factor
HYMD1326458-H	VDD=2.5V VDDQ=2.5V	133MHz (*DDR266B)	SSTL_2	184pin Unbuffered DIMM 5.25 x 1.25 x 0.15 inch
HYMD1326458-L		100MHz (*DDR200)		

** JEDEC Defined Specifications compliant*

This document is a general product description and is subject to change without notice. Hynix Semiconductor does not assume any responsibility for use of circuits described. No patent licenses are implied.

PIN DESCRIPTION

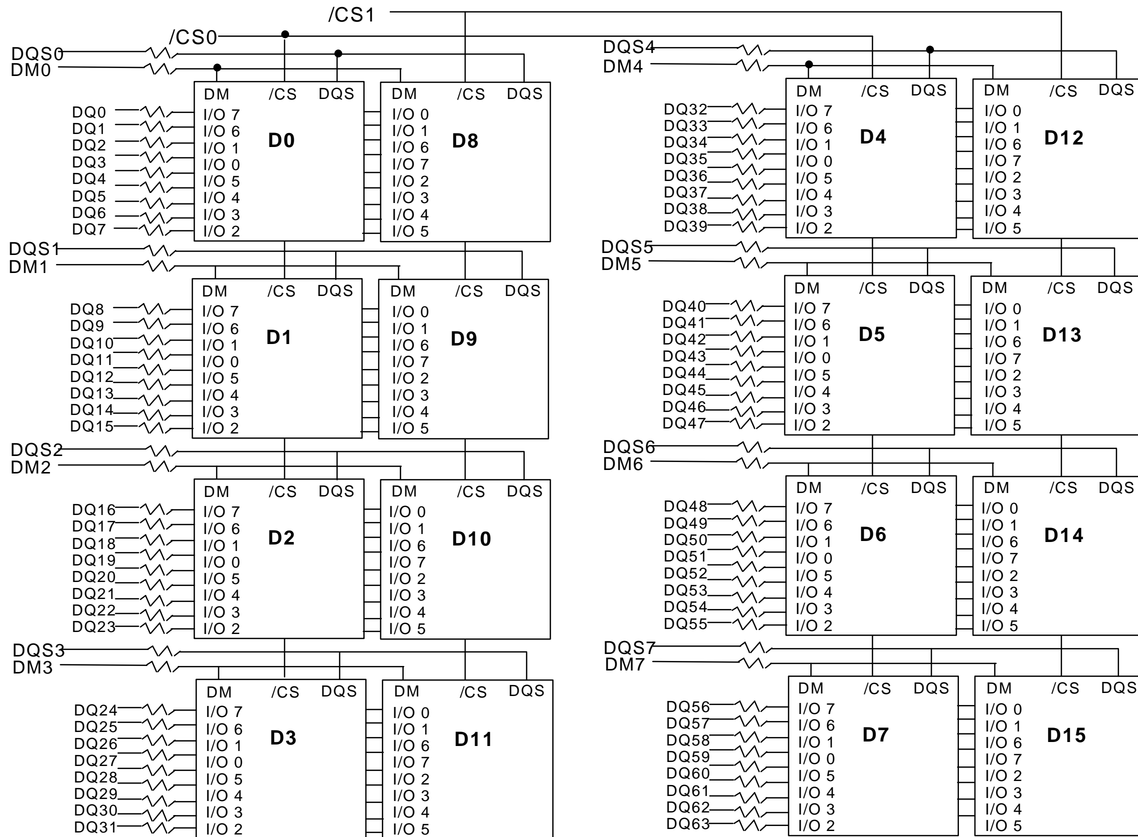
Pin	Pin Description	Pin	Pin Description
CK0,/CK0,CK1,/CK1,CK2,/CK2	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0, CS1	Chip Select Input	VSS	Ground
CKE0, CKE1	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAS, /WE	Commend Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A11	Address	SA0~SA2	E^2PROM Address Inputs
BA0, BA1	Bank Address	SCL	E^2PROM Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	E^2PROM Data I/O
DQS0~DQS7	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0~DM7	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection

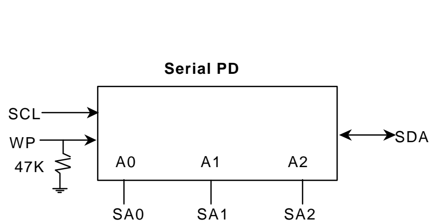
PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	Vss	72	DQ48	103	A13*	134	CB4*	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5*	165	DQ52
13	DQ9	44	CB0*	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1*	75	/CK2	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	DQS8*	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	DM8*	170	DQ54
18	VSS	49	CB2*	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6*	172	VDDQ
20	DQ11	51	CB3*	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7*	174	DQ60
22	VDDQ	Key		83	DQ56	114	DQ20	key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12*	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	WP	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

* These are not used on this module but may be used for other module in 184pin DIMM family

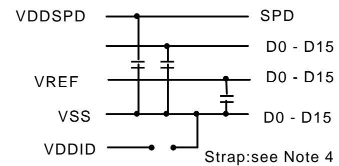
FUNCTIONAL BLOCK DIAGRAM





*Clock Wiring	
Clock Input	SDRAMs
*CK0,/CK0 *CK1,/CK1 *CK2,/CK2	4 SDRAMs 6 SDRAMs 6 SDRAMs

* Wire per clock loading table/wiring diagrams



BA0-BA1 → BA0-BA1 : SDRAMs D0 - D15
A0 - A11 → A0 - A11 : SDRAMs D0 - D15
CKE1 → CKE1 : SDRAMs D8 - D15
/RAS → /RAS : SDRAMs D0 - D15
/CAS → /CAS : SDRAMs D0 - D15
CKE0 → CKE : SDRAMs D0 - D7
/WE → /WE : SDRAMs D0 - D15

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown
3. DQ, DQS, DM/DQS resistors : 22Ohms+/-5%
4. VDDID strap connections (for memory device VDD, VDDQ) :
   Strap out :(open) : VDD=VDDQ
   Strap In (Vss) : VDD≠ VDDQ

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	16	W
Soldering Temperature / Time	TSOLDER	260 / 10	°C / Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS=0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD	2.3	2.5	2.7	V	
Power Supply Voltage	VDDQ	2.3	2.5	2.7	V	1
Input High Voltage	VIH	VREF + 0.15	-	VDDQ + 0.3	V	
Input Low Voltage	VIL	-0.3	-	VREF - 0.15	V	2
Termination Voltage	VTT	VREF - 0.04	VREF	VREF + 0.04	V	
Reference Voltage	VREF	1.15	1.25	1.35	V	3

Note :
1. VDDQ must not exceed the level of VDD.
2. VIL(min) is acceptable -1.5V AC pulse width with $\leq$ 5ns of duration.
3. The value of VREF is approximately equal to 0.5VDDQ.

AC OPERATING CONDITIONS (TA=0 to 70 °C, Voltage referenced to VSS=0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL(AC)		VREF - 0.31	V	
Input Differential Voltage, CK and /CK inputs	VID(AC)	0.7	VDDQ + 0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note :
1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

AC OPERATING TEST CONDITIONS (TA=0 to 70°C, Voltage referenced to VSS=0V)

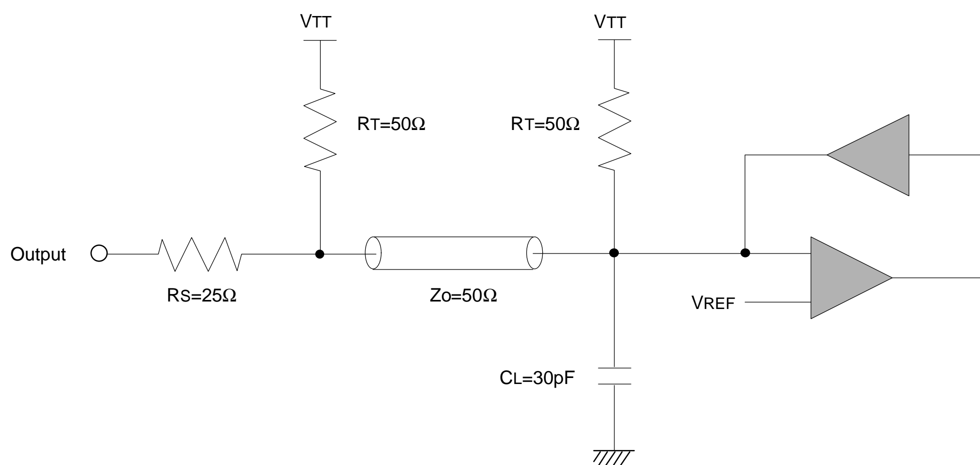
Parameter	Value	Unit
Reference Voltage	VDDQ x 0.5	V
Termination Voltage	VDDQ x 0.5	V
AC Input High Level Voltage (VIH, min)	VREF + 0.31	V
AC Input Low Level Voltage (VIL, max)	VREF - 0.31	V
Input Timing Measurement Reference Level Voltage	VREF	V
Output Timing Measurement Reference Level Voltage	VTT	V
Input Signal maximum peak swing	1.5	V
Input minimum Signal Slew Rate	1	V/ns
Termination Resistor (RT)	50	Ω
Series Resistor (RS)	25	Ω
Output Load Capacitance for Access Time Measurement (CL)	30	pF

CAPACITANCE (TA=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A11, BA0, BA1	CIN1	93	107	pF
Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CIN2	93	107	pF
Input Capacitance	CKE0, CKE1	CIN3	63	77	pF
Input Capacitance	CS0, CS1	CIN4	58	72	pF
Input Capacitance	CK0, $\overline{CK0}$, CK1, $\overline{CK1}$, CK2,$\overline{CK2}$	CIN5	30	45	pF
Input Capacitance	DM0 ~ DM7	CIN6	10	15	pF
Data Input / Output Capacitance	DQ0 ~ DQ63, DQS0 ~ DQS7	CIO1	10	15	pF

Note :
1. VDD=min. to max., VDDQ=2.3V to 2.7V, VODC=VDDQ/2, VOpeak-to-peak=0.2V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



DC CHARACTERISTICS I (TA=0 to 70°C, Voltage referenced to VSS=0V)

Parameter	Symbol	Min.	Max	Unit	Note
Input Leakage Current	ILI	-5	5	uA	1
Output Leakage Current	ILO	-5	5	uA	2
Output High Voltage	VOH	VTT + 0.76	-	V	IOH = -15.2mA
Output Low Voltage	VOL	-	VTT - 0.76	V	IOL = +15.2mA

Note :
1. VIN=0 to 3.6V, All other pins are not tested under VIN=0V
2. DOUT is disabled, VOUT=0 to 2.7V
3. These values are device characteristics.

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS=0V)

Parameter	Symbol	Test Condition	Speed		Unit	Note
			-H	-L		
Operating Current	IDD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	TBD	TBD	mA	
Operating Current	IDD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	2240	2080	mA	
Precharge Power Down Standby Current	IDD2P	All banks idle; Power down - mode; CKE=Low, tCK=tCK(min)	320		mA	
Idle Standby Current	IDD2F	$\overline{CS}$=High, All banks idle; tCK=tCK(min); CKE=High; address and control inputs changing once per clock cycle. VIN=VREF for DQ, DQS and DM	320	280	mA	
Active Power Down Standby Current	IDD3P	One bank active; Power down mode; CKE=Low, tCK=tCK(min)	400		mA	
Active Standby Current	IDD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge; tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	800		mA	

DC CHARACTERISTICS II (TA=0 to 70°C, Voltage referenced to VSS=0V)

- Continued-

Parameter	Symbol	Test Condition		Speed		Unit	Note
				-H	-L		
Operating Current	IDD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA		TBD	TBD	mA	
Operating Current	IDD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle		TBD	TBD	mA	
Auto Refresh Current	IDD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh		5120		mA	
Self Refresh Current	IDD6	CKE=< 0.2V; External clock on; tCK=tCK(min)	Normal	32		mA	
			Low Power	16		mA	
Operating Current - Four Bank Operation	IDD7	Four bank interleaving with BL=4, Refer to the following page for detailed test condition		TBD		mA	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-H(DDR266B)		-L(DDR200)		Unit	Note
			Min	Max	Min	Max		
Row Cycle Time		tRC	65	-	70	-	ns	
Auto Refresh Row Cycle Time		tRFC	75	-	80	-	ns	
Row Active Time		tRAS	45	120K	50	120K	ns	
Active to Read with Auto Precharge Delay		tRAP	tRAS-BL/2 x tCK	-	tRAS-BL/2 x tCK	-	ns	16
Row Address to Column Address Delay		tRCD	20	-	20	-	ns	
Row Active to Row Active Delay		tRRD	15	-	15	-	ns	
Column Address to Column Address Delay		tCCD	1	-	1	-	CK	
Row Precharge Time		tRP	20	-	20	-	ns	
Last Date-In to Precharge Time (Write Recovery Time)		tDPL	15	-	20	-	ns	
Last Data-In to Read Command		tDRL	1	-	1	-	CK	
Auto Precharge Write Recovery + Precharge Time		tDAL	5	-	4	-	CK	15
System Clock Cycle Time	CL = 2.5	tCK	7.5	15	10	15	ns	
	CL = 2		10	15	10	15	ns	
Clock High Level Width		tCH	0.45	0.55	0.45	0.55	CK	
Clock Low Level Width		tCL	0.45	0.55	0.45	0.55	CK	
Data-Out edge to Clock edge Skew		tAC	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Clock edge Skew		tDQSCK	-0.75	0.75	-0.8	0.8	ns	
DQS-Out edge to Data-Out edge Skew		tDQSQ	-	0.5	-	0.6	ns	
Data-Out hold time from DQS		tQH	tHPmin -tQHS	-	tHPmin -tQHS	-	ns	1, 10
Clock Half Period		tHP	tCH/L min	-	tCH/L min	-	ns	1,9
Data Hold Skew Factor		tQHS	-	0.75	-	1	ns	10
Valid Data Output Window		tDV	tQH-tDQSQ		tQH-tDQSQ		ns	
Data-out high-impedance window from CK, /CK		tHZ			-1.2	0.8	ns	
Data-out low-impedance window from CK, /CK		tLZ			-1.2	0.8	ns	
Input Setup Time (fast slew rate)		tIS	0.9	-	1.2	-	ns	2,3,5,6
Input Hold Time (fast slew rate)		tIH	0.9	-	1.2	-	ns	2,3,5,6
Input Setup Time (slow slew rate)		tIS	1.0	-	1.2	-	ns	2,4,5,6
Input Hold Time (slow slew rate)		tIH	1.0	-	1.2	-	ns	2,4,5,6
Input Pulse Width		tIPW	2.2		-		ns	6
Write DQS High Level Width		tDQSH	0.35	-	0.35	-	CK	

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

- continued -

Parameter	Symbol	-H(DDR266B)		-L(DDR200)		Unit	Note
		Min	Max	Min	Max		
Write DQS Low Level Width	tDQSL	0.35	-	0.35	-	CK	
Clock to First Rising edge of DQS-In	tDQSS	0.75	1.25	0.75	1.25	CK	
Data-In Setup Time to DQS-In (DQ & DM)	tDS	0.5	-	0.6	-	ns	6,7, 11~13
Data-in Hold Time to DQS-In (DQ & DM)	tDH	0.5	-	0.6	-	ns	6,7, 11~13
DQ & DM Input Pulse Width	tDIPW	1.75	-	2	-	ns	
Read DQS Preamble Time	tRPRE	0.9	1.1	0.9	1.1	CK	
Read DQS Postamble Time	tRPST	0.4	0.6	0.4	0.6	CK	
Write DQS Preamble Setup Time	tWPRES	0	-	0	-	CK	
Write DQS Preamble Hold Time	tWPREH	0.25	-	0.25	-	CK	
Write DQS Postamble Time	tWPST	0.4	0.6	0.4	0.6	CK	
Mode Register Set Delay	tMRD	2	-	2	-	CK	
Exit Self Refresh to Any Execute Command	tXSC	200	-	200	-	CK	8
Average Periodic Refresh Interval	tREFI	-	15.6	-	15.6	us	

Note :

1. This calculation accounts for tDQSQ(max), the pulse width distortion of on-chip circuit and jitter.
2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
3. For command/address input slew rate >=1.0V/ns
4. For command/address input slew rate >=0.5V/ns and <1.0V/ns
   This derating table is used to increase tIS/tIH in case where the input slew-rate is below 0.5V/ns.
   Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tIS	Delta tIH
V/ns	ps	ps
0.5	0	0
0.4	+50	0
0.3	+100	0

5. CK, /CK slew rates are >=1.0V/ns
6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
7. Data latched at both rising and falling edges of Data Strobes(LDQS/UDQS) : DQ, LDM/UDM.
8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete SelfRefresh Exit and lock the internal DLL circuit of DDR SDRAM.
9. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH).
10. tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS consists of tDQSQmax, the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

11. This derating table is used to increase tDS/tDH in case where the input slew-rate is below 0.5V/ns.

Input Setup / Hold Slew-rate Derating Table.

Input Setup / Hold Slew-rate	Delta tDS	Delta tDH
V/ns	ps	ps
0.5	0	0
0.4	+75	+75
0.3	+150	+150

12. I/O Setup/Hold Plateau Derating. This derating table is used to increase tDS/tDH in case where the input level is flat below VREF +/-310mV for a duration of up to 2ns.

I/O Input Level	Delta tDS	Delta tDH
mV	ps	ps
+280	+50	+50

13. I/O Setup/Hold Delta Inverse Slew Rate Derating. This derating table is used to increase tDS/tDH in case where the DQ and DQS slew rates differ. The Delta Inverse Slew Rate is calculated as (1/SlewRate1)-(1/SlewRate2). For example, if slew rate1=0.5V/ns and Slew Rate2=0.4V/n then the Delta Inverse Slew Rate=-0.5ns/V.

(1/SlewRate1)-(1/SlewRate2)	Delta tDS	Delta tDH
ns/V	ps	ps
0	0	0
+/-0.25	+50	+50
+/- 0.5	+100	+100

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transi tions through the DC region must be monotonic.

15. tDAL=(tDPL / tCK) + (tRP / tCK). For each of the terms above, if not already an integer, round to the next highest integer. tCK is equal to the actual system clock cycle time.
Example: For DDR266B at CL=2.5 and tCK=7.5 ns,
tDAL=(15 ns / 7.5 ns) + (20 ns / 7.5 ns)=(2.00) + (2.67)
Round up each non-integer to the next highest integer:=(2) + (3), tDAL=5 clocks

16. For the parts which do not has internal RAS lockout circuit, Active to Read with Auto precharge delay should be tRAS - BL/2 x tCK.

SIMPLIFIED COMMAND TRUTH TABLE

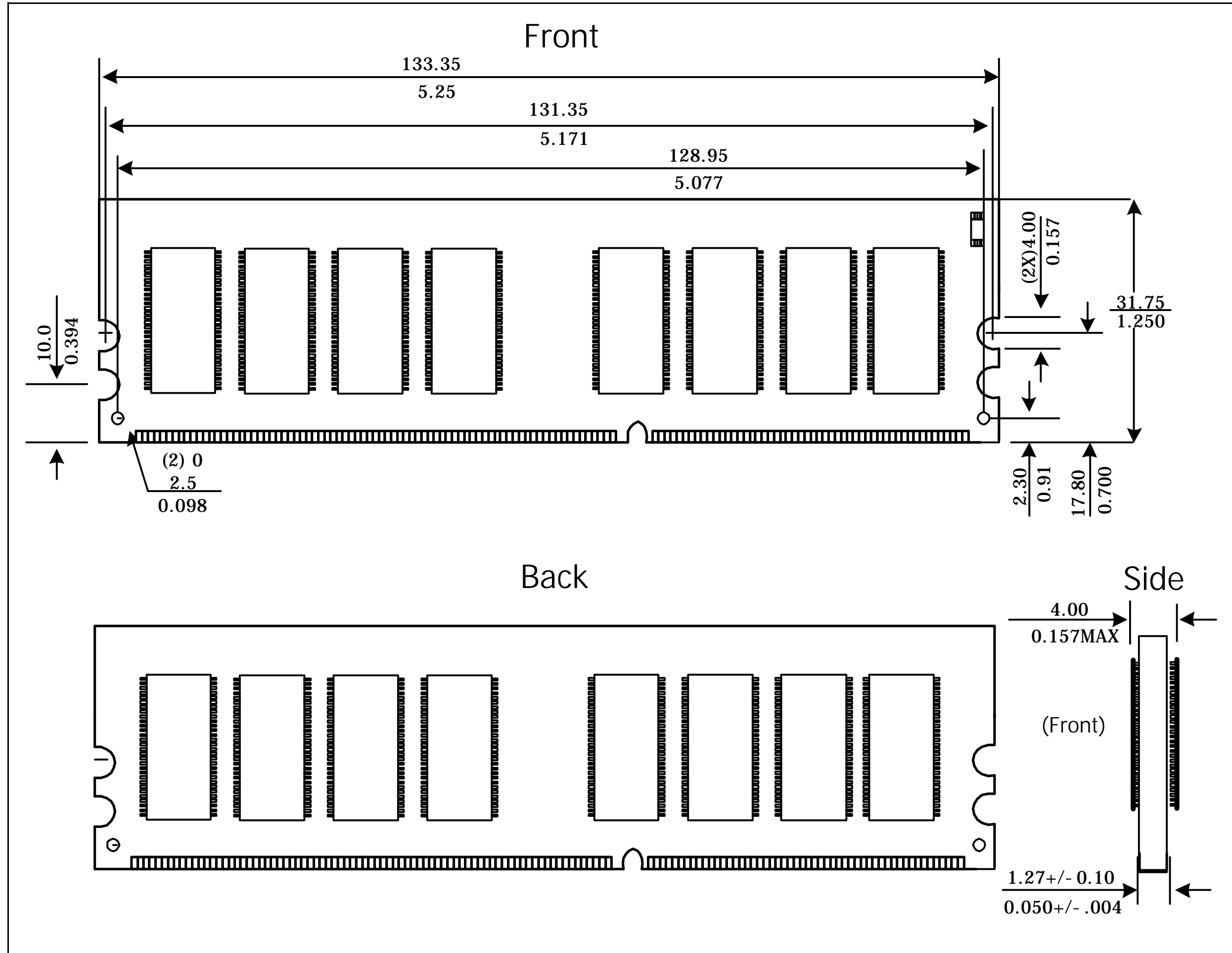
Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	A10/AP	BA	Note
Extended Mode Register Set		H	X	L	L	L	L	OP code			1,2
Mode Register Set		H	X	L	L	L	L	OP code			1,2
Device Deselect		H	X	H	X	X	X	X			1
No Operation				L	H	H	H				
Bank Active		H	X	L	L	H	H	RA		V	1
Read		H	X	L	H	L	H	CA	L	V	1
Read with Autoprecharge									H		1,3
Write		H	X	L	H	L	L	CA	L	V	1
Write with Autoprecharge									H		1,4
Precharge All Banks		H	X	L	L	H	L	X	H	X	1,5
Precharge selected Bank									L	V	1
Read Burst Stop		H	X	L	H	H	L	X			1
Auto Refresh		H	H	L	L	L	H	X			1
Self Refresh	Entry	H	L	L	L	L	H	X			1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	H	H	H				1
	Exit	L	H	H	X	X	X				1
				L	H	H	H				1
Active Power Down Mode	Entry	H	L	H	X	X	X	X			1
				L	V	V	V				1
	Exit	L	H	X							1

(H=Logic High Level, L=Logic Low Level, X=Dont Care, V=Valid Data Input, OP Code=Operand Code, NOP=No Operation)

Note :

1. DM states are Don't Care. Refer to below Write Mask Truth Table.
2. OP Code(Operand Code) consists of A0~A11 and BA0~BA1 used for Mode Registering duing Extended MRS or MRS.
   Before entering Mode Register Set mode, all banks must be in a precharge state and MRS command can be issued after tRP period from Prechagre command.
3. If a Read with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+tRP).
4. If a Write with Autoprecharge command is detected by memory component in CK(n), then there will be no command presented to activated bank until CK(n+BL/2+1+tDPL+tRP). Last Data-In to Prechage delay(tDPL) which is also called Write Recovery Time (tWR) is needed to guarantee that the last data has been completely written.
5. If A10/AP is High when Row Precharge command being issued, BA0/BA1 are ignored and all banks are selected to be precharged.

PACKAGE DIMENSIONS



SPD SPECIFICATION

(32Mx64 DDR SDRAM Unbuffered DIMM)

Based on 16Mx8 DDR SDRAM with SSTL_2, 4Banks & 4K Refresh

SERIAL PRESENCE DETECT

Bin Sort : K(DDR266A@CL=2), H(DDR266B@CL=2.5), L(DDR200@CL=2)

Byte#	Function Description	Function Supported			Hexa Value			Note
		K	H	L	K	H	L	
0	Number of Bytes written into serial memory at module manufacturer	128 Bytes			80h			
1	Total number of Bytes in SPD device	256 Bytes			08h			
2	Fundamental memory type	DDR SDRAM			07h			
3	Number of row address on this assembly	12			0Ch			1
4	Number of column address on this assembly	10			0Ah			1
5	Number of physical banks on DIMM	2Bank			02h			
6	Module data width	64 Bits			40h			
7	Module data width (continued)	-			00h			
8	Module voltage Interface levels(VDDQ)	SSTL 2.5V			04h			
9	DDR SDRAM cycle time at CAS Latency=2.5(tCK)	7.5ns	7.5ns	10ns	75h	75h	A0h	2
10	DDR SDRAM access time from clock at CL=2.5 (tAC)	+/-0.75ns	+/-0.75ns	+/-0.8ns	75h	75h	80h	2
11	Module configuration type	Non-ECC			00h			
12	Refresh rate and type	15.6us & Self refresh			80h			
13	Primary DDR SDRAM width	x8			08h			
14	Error checking DDR SDRAM data width	N/A			00h			
15	Minimum clock delay for back-to-back random column address(tCCD)	1 CLK			01h			
16	Burst lengths supported	2,4,8			0Eh			
17	Number of banks on each DDR SDRAM	4 Banks			04h			
18	CAS latency supported	2, 2.5			0Ch			
19	CS latency	0			01h			
20	WE latency	1			02h			
21	DDR SDRAM module attributes	differential clock input			20h			
22	DDR SDRAM device attributes : General	+/-0.2Voltage tolerance			00h			
23	DDR SDRAM cycle time at CL=2.0(tCK)	7.5ns	10ns	10ns	75h	A0h	A0h	
24	DDR SDRAM access time from clock at CL=2.0(tAC)	+/-0.75ns	+/-0.75ns	+/-0.8ns	75h	75h	80h	
25	DDR SDRAM cycle time at CL=1.5(tCK)	-			00h			
26	DDR SDRAM access time from clock at CL=1.5(tAC)	-			00h			
27	Minimum row precharge time(tRP)	20ns	20ns	20ns	50h	50h	50h	
28	Minimum row activate to row active delay(tRRD)	15ns	15ns	15ns	3Ch	3Ch	3Ch	
29	Minimum RAS to CAS delay(tRCD)	20ns	20ns	20ns	50h	50h	50h	
30	Minimum active to precharge time(tRAS)	45ns	45ns	50ns	2Dh	2Dh	32h	
31	Module row density	128MB			20h			
32	Command and address signal input setup time(tIS)	0.9ns	0.9ns	1.2ns	90h	90h	C0h	
33	Command and address signal input hold time(tIH)	0.9ns	0.9ns	1.2ns	90h	90h	C0h	
34	Data signal input setup time(tDS)	0.5ns	0.5ns	0.6ns	50h	50h	60h	
35	Data signal input hold time(tDH)	0.5ns	0.5ns	0.6ns	50h	50h	60h	

SERIAL PRESENCE DETECT(continued)

Byte #	Function Description	Function Supported			Hexa Value			Note
		K	H	L	K	H	L	
36~61	Superset information(may be used in future)	-			00h			
62	SPD Revision code	Initial release			00h			
63	Checksum for Bytes 0~62	-			72h	9Dh	63h	
64	Manufacturer JEDEC ID Code	Hynix JEDEC ID			ADh			
65~71	--------- Manufacturer JEDEC ID Code	-			00h			
72	Manufacturing location	Hynix(Korea Area) HSA(United States Area) HSE(Europe Area) HSJ(Japan Area) Singapore Asia Area			0*h 1*h 2*h 3*h 4*h 5*h			6
73	Manufacture part number(Hynix Memory Module)	H			4Dh			
74	--------Manufacture part number(Hynix Memory Module)	Y			48h			
75	--------Manufacture part number(Hynix Memory Module)	M			59h			
76	Manufacture part number (DDR SDRAM)	D			44h			
77	Manufacture part number(Memory density)	1			31h			
78	Manufacture part number(Module Depth)	3			33h			
79	------- Manufacture part number(Module Depth)	2			32h			
80	Manufacture part number(Module type)	Blank			20h			
81	Manufacture part number(Data width)	6			36h			
82	-------Manufacture part number(Data width)	4			34h			
83	Manufacture part number(Refresh, # of Bank.)	5(4K refresh,4Bank)			35h			
84	Manufacture part number(Component configuration)	8			38h			
85	Manufacture part number(Hyphen)	'-'			2Dh			
86	Manufacture part number(Minimum cycle time)	K	H	L	4Bh	48h	4Ch	
87~90	Manufacture part number(T.B.D)	Blank			20h			
91	Manufacture revision code(for Component)	Blank			20h			
92	Manufacture revision code (for PCB)	0			30h			
93	Manufacturing date(week)	-			-			3
94	Manufacturing date(Year)	-			-			3
95~98	Module serial number	-			-			4
99~127	Manufacturer specific data (may be used in future)	Undefined			00h			5
128~255	Open for customer use	Undefined			00h			5

Note :

1. The bank address is excluded
2. These value is based on the component specification
3. These bytes are programmed by code of date week & date year
4. These bytes apply to Hynix's own Module Serial Number system
5. These bytes undefined and coded as '00h'
6. Refer to Hynix web site