

PowerPC™

Application Note

MPC860 Board Design Checklist

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Introduction

When integrating MPC8xx family members into an application, it may be helpful to go through the following design checklist. This checklist outlines a number of common problems with respective solutions that have been found while debugging real MPC860 applications.

Checklist

Version, Mask

The first version of the MPC860 was called rev 0. Metal fixes were made to this version to create versions such as rev 0.1. The first full layer change was revision A. Subsequent metal fixes add numbers to the revision, such as A.2.

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Choosing Oscillators versus Crystals

If you can afford the power dissipation of using an oscillator rather than a crystal, choose an oscillator. Crystal circuits must often be tweaked after the die goes through a geometry shrink.

Using both Oscillators and Crystals

Crystal oscillators and crystals can be used together on the MPC860, however do not use the crystal on the EXTAL and XTAL pins and leave the oscillator free-running into the EXTCLK pin as this will cause excessive jitter. Rather, externally gate the clock of the oscillator to the EXTCLK pin while the crystal is in use. It's good design practice that if you're not using a crystal, ground the EXTAL pin.

Clock Circuit Layout

Locate the crystal within 0.5 inches of the MPC8xx. The closer the better. The XFC capacitor should be physically as close as possible to the MPC8xx as well.

VDDsyn Filter

Use a LC filter on the VDDsyn pin instead of a RC filter. Please refer to the MPC860ADS schematic for a good example of a proper circuit.

5 Volt Friendly Signals

Although the MPC8xx does support 5V inputs, please note that EXTAL and EXTCLK are not 5 Volt friendly inputs. Inputs on those signals are limited to 3.3V.

Power Supply 2.2V Confusion

Connect 3.3V to the internal logic VCC pins (called VDDL) and all other power pins on the MPC8xx and not 2.2V. The use of 2.2V on VDDL was illustrated in one of the example user manual drawings, but is only allowed if a special version of the MPC8xx is purchased. At the time of writing this document, this special 2.2V version had not been introduced, so be sure to check with your local Motorola representative for availability, if this mode is required.

Memory, DRAM

Not all DRAM SIMMs are created equal. With Motorola SIMMs the signal integrity on the DRAM control and address lines look good. With other manufacturers, series damping resistors need to be used. The MPC860ADS board was designed for Motorola SIMMs, and therefore does not show series damping resistors.

Memory, DRAM, External Master

If an external master device is accessing DRAM using the MPC8xx memory controller, the burst address pins (BADDR(28:30)) on the MPC8xx should be connected through the multiplexer, and not directly to the DRAM.

How Many Layer Board?

It is recommended to use one ground plane, one 3.3V VCC plane, and one 5.0V VCC plane (if 5V parts exist in the system). In addition at least four signal planes would normally be used to ensure easy routing to/from the MPC860.

Analog Power Supply

The MPC860ADS board design pays particular attention to the power planes in the area of the PLL power. The VDDsyn pin is routed to a via that punches down to a mini plane (really a peninsula on a signal layer) which is decoupled from VSSsyn with 10UF and 0.1UF parallel caps and also attaches to the 3.3 Volt plane through a 8.2mH inductor. The 3.3 and 5 volt planes have a keepout in the PLL power area. Separate the PLL VSSsyn from Global ground by means of a split in the plane with a connection point as close to the supply as possible. On other layers, signals are kept out of this area. Also, the PLL loop filter and decoupling caps should be placed as close to the MPC8xx as possible.

Pullups on the Data Bus

Putting pullups on the Data Bus has implications on the initial configuration of the MPC8xx, since there is a mode whereby the part could sample the data bus during reset to determine its initial configuration. If you choose to put pullups on the data bus, make sure that the RSTCONF* pin is tied high, otherwise the default MPC8xx configuration values will be overwritten with ones from the pullups on the data bus. Alternatively, you can put pullups on the data bus (for the purpose of using them as bus keeps), if you drive all of the configuration pins actively high or low (as appropriate) during reset, as described below. The pullups can be terminated to either 5 or 3.3 volts and the value is left up to the designer.

Hard Reset Configuration Word Pins

The data bus is sampled at reset to determine the initial configuration of the MPC8xx if the RSTCONF* pin is tied low. Ensure that the correct values are driven to the bus during the PORESET and HRESET periods. For any data pins that the user wishes to configure as 1's (i.e. where the default configuration is not appropriate), do not expect pullups to be sufficient. Use active drivers to drive 1's and 0's if pullups are already being used on the data bus. The drivers should then be disabled following reset.

Powerup Reset Circuit

There is no power up detector on the MPC8xx like there was on the 68360. To construct a simple circuit, hang a diode, cap and resistor network on PORESET line. A more robust (expensive) solution is to use a power on reset chip monitoring the power plane. Hard reset is a bidirectional signal and if used, needs to be driven with an open collector (open drain) device. Diodes should be used on the reset inputs to cause

sharp transitions of those signals. The 860ADS board has an excellent treatment of the reset circuit, and should be followed as a guide.

MPC860 Driving SRESET*

The MPC8xx can drive the soft reset pin (SRESET*) as an output. It is driven by the MPC8xx any time that the PORESET* lines or the HRESET* line is asserted and also if a RESET command is delivered to the debug port.

So You Need a Halt Signal?

The MPC860 does not support a Halt signal. One suggestion we can make for board designers that have to have one, is to monitor the AT3-0 pins for an absence of activity.

MODCK Pins

The MODCK pins become outputs after reset. To configure them, drive them with three state buffers enabled with HRESET*. Although MODCK is latched on rising edge of PORESET*, this is a slow edge so use HRESET* as the enable.

Byte Lane for Boot EPROM

If eight bit wide memory/EPROM is used, attach the device to byte lane zero (D0-D7). Note that in PowerPC terminology, D0-D7 is the highest order byte lane on the data bus, and D0 is the highest order pin of that byte lane. D0-D7 corresponds to write enable 0 (WE0*) and Byte Select A or B 0 (e.g. BS_A0*).

D0-D7 --> WE0* --> BS_B0* or BS_A0*

D15-D8 --> WE1* --> BS_B1* or BS_A1*

D23-D16 --> WE2* --> BS_B2* or BS_A2*

D31-D24 --> WE3* --> BS_B3* or BS_A3*

Highest order data pin: D0. Lowest order data pin: D31.

Address Pins

The highest order address pin is A0. The lowest order address pin is A31. Check that the MSB (0) and LSB (31) are correctly connected. In a byte access, all 32 address pins are valid. In a 32-bit word access, only the upper 30 address pins are used (A0-29). A30 and A31 should both be zero.

Address/Data Nomenclature

We recommend that you build your schematics in accordance with the PowerPC terminology. If you try to "rename" your address or data bus pins to make them 68K friendly (e.g. by renaming A0 to be A31), you will probably end up with mistakes on your board design.

Chip Select Double Drive

It is possible to get more drive capability on CS2* and CS3* by having these signals output on 2 pins each. CS2* can be driven on the normal CS2* pin and GPL_A2*. CS3* can be driven on the normal CS3* pin and also GPL_A3*. Note that the CS* pins can also be used as RAS* lines, where drive capability often is critical in gaining the last nanosecond from the memory system. The double drive capability is programmed in the SIUMCR.

Be Careful of R/W*

A R/W* pin is provided on the chip, but its timing is not appropriate for all memory types. Remember that the R/W* timing is fixed, and the WE0-3* signals are usually a better choice. If the WE0-3* signal timing is not suitable, the more flexible UPM machine of the memory controller can be used to give precise timings on these signals.

Put a 10-pin Header for the Development Port on Your Board

The Development Port section of the user's manual describes a 10-pin header that should be included on your board. Physically locate the 10 pin connector as close as possible to the processor to minimize trace length and cross coupling of noise onto the BDM signals. Do not run high speed clocks or signals adjacent to the BDM communication signals. When your boards arrive, you can begin initial testing via this port. The MPC860ADS board describes a feature whereby you can connect your 10-pin header to another 10-pin header on our ADS board. By connecting our ADS board to a PC, you can use our PC hosted debugger to begin to manipulate registers on the target board, just as you would on our ADS board. (Remember that the MPC8xx device on the ADS board must be removed for this mode of operation, and use the shortest possible cable between the ADS and your target). In addition, other third-party tools use this 10-pin header for their debugger capability.

Debug Port Interface

The DSDI and DSCK pins are configured during reset to select certain modes of the development port system interface. If the user wishes to pull the DSCK pin low, then a 1Kohm pulldown should be used to make sure that low logic levels are recognized on all versions of the MPC8xx. DSDI should have a pullup to be on the safe side (there is an internal pullup). For the TA*, TEA* and BB* signal pins, use a 1k ohm pull-up resistor. If not you will get erratic operation.

PCMCIA Buffers Not Needed

Although the MPC8xx manual shows buffers in the PCMCIA design example, it is noted that such buffers on the address or data bus are only required if the address or data bus is heavily loaded, a 2 PCMCIA slot system is designed, or the board requires protection from hot plug-in of PCMCIA cards.

IDMA, Memory-to-Memory

If the user desires to use the IDMA in memory-to-memory mode, the DREQ* pin must be asserted. It is possible to ground the pin or use a parallel I/O pin to selectively enable the DREQ* function. Using the parallel I/O pin is preferable, to save the added overhead of the CPM RISC polling the IDMA buffer descriptors to see if the valid bit has been set.

Port Pins, Pullups

The parallel port pins on the MPC860 do not have internal pullups or pulldowns. Unused parallel I/O pins may be configured as outputs after reset and left unconnected.

Unused Input Pins

Unused inputs should be tied high or low, but not left floating. Unused inputs may be tied directly to VCC or GND or through pullups or pulldowns to VCC or GND. For most pins, VCC can be either 3.3V or 5.0V.

Unused Output Pins

Unused output pins may be left unconnected.

Erratic device operation following power up

Ensure the TRST signal is connected as recommended in the rev. 1 version of the users manual as follows:

If both the TAP (Test Access Port) and low power mode are NEVER used, connect TRST to ground. If the TAP or low power mode is used, connect TRST to PORESET. If power down mode (the lowest power mode, where Vddh is disabled) is used, connect TRST to PORESET through a diode (anode to TRST, cathode to PORESET). Do NOT connect TRST to HRESET as was previously recommended in certain documentation.

Additional information on these areas is detailed in the Rev.1 version of the MPC860 Users Manual (UM). Please review sections 13.3 and 13.4 for full details.

Controlling Excessive Rise Time on Negation of PORESET*

To control excessive rise time on negation of PORESET* with an emulator installed, pullup the PORESET* line with a 1-K ohm pullup resistor.

Using an 860T or 860EN:

Locate the processor and ethernet controller as physically close together as is feasible. Provide for a series resistor option to fine tune clock ringing on RCLK and TCLK.

UPM Design Hint When Using an Emulator

It may be necessary to change UPM values when using a non-DPI (Debug Port Interface) connection method because of the impedance impact of installing an emulator probe or other line loading device into a target.

Easier Testing/Debugging Hint

Wherever possible place pads on the opposite side of the board from the processor for a possible future mirror probe connection.

MPC850 and MPC823 external masters

The 850 and 823 have only 26 externally visible address bits. Therefore, external masters should only address the range from hex 0000 0000 to x3FF FFFF if the external master uses the memory controller or any of it's functions on the 850/823. The bits from an external master will be seen as 0's by the memory controller. Internally the address bits are present and can be addressed for MMU and cache functions from the PPC core.

CLKOUT Signal

The drive capability of the CLKOUT signal is modest. If necessary, use a clock driver/distribution device to redrive this signal. The MPC974 ,for example, can be configured as a (near) zero delay buffer.

PLL

Loop filter values require careful selection, and placement. Power Supply decoupling for the PLL requires attention as well.

Chip Select 0

Ensure that CS0 is connected to the boot memory device.

Using FLASH Devices


Ensure the correct FLASH bit ordering for the correct programming algorithm is connected.

HRESET*, SRESET*, PORESET*, and TA* Signals

Provide low resistance value pull-ups (1K to 4.7 K) on the following signals: HRESET*, SRESET*, PORESET*, and TA*.

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