2Mx64 3.3V Simultaneous Operation Multi-Chip Package *Preliminary

FEATURES

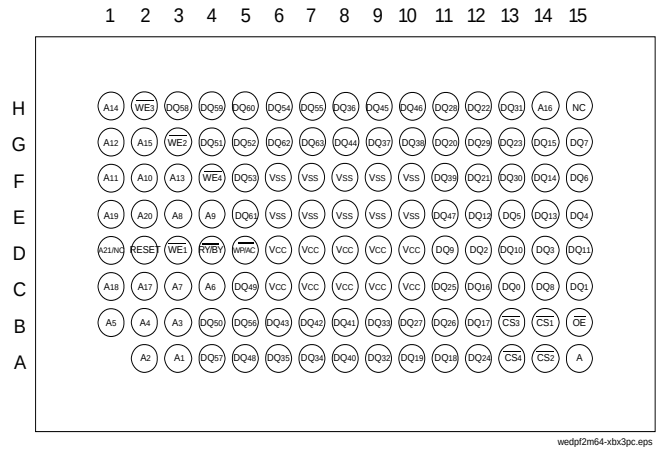
- Access Times of 70, 100, 120, 150ns
- Packaging
  - 119 ball stacked TSOP BGA
- 1,000,000 Erase/Program Cycles
- Sector Architecture
  - 252 32K word sectors and 32 4K word sectors
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 2Mx64
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Simultaneous Read/Write Operation
  - Data can be continuously read from one bank while executing erase/program functions in other banks
- Embedded Erase and Program Algorithms
- $\overline{\text{Erase}}$ Suspend/Resume
  - Supports reading data from or programing data to a sector not being erased
- Data Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
  - Reduces overall programming time when issuing multiple program command sequences
- Ready/$\overline{\text{Busy}}$ output (RY/$\overline{\text{BY}}$)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method of resetting the internal state machine to the read mode
- $\overline{\text{WP}}$/ACC input pin
  - Write protect ($\overline{\text{WP}}$) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector Protection
  - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

Note: For programming information refer to Flash Programming WEDPF2M64-XXX3 Application Note.

** Preliminary datasheet. This datasheet describes a product that is not fully qualified or characterized and is subject to change without notice.*

FIG 1: PIN CONFIGURATION FOR WEDPF2M64-XBX3

TOP VIEW

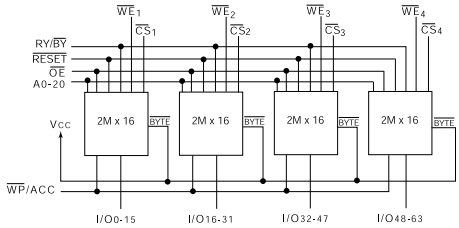


wedpf2m64-xbx3pc.eps

PIN DESCRIPTION

I/O0-63	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RESET}$	Reset/Powerdown
Vcc	Power Supply
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Storage Temperature Range	-65 to +150	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	0.7 x Vcc	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE
(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	8	pF
CS_{1-4} capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	10	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	12	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	25	pF
$\overline{RESET}$ capacitance	C_{RS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
RY/$\overline{BY}$ capacitance	C_{RB}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{WP}$/AC capacitance	C_{WA}	V_{IN} = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS - CMOS COMPATIBLE
(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 3.6, V_{IN} = GND or V_{CC}				10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 3.6, V_{IN} = GND or V_{CC}				10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz				65	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}				120	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 3.6, CS = V_{IH}, f = 5MHz				20	mA
V_{CC} Reset Current (2)	I_{CC4}	$\overline{RESET}$ = V_{SS} ± 0.3V			1	20	mA
Automatic Sleep Mode (2,4)	I_{CC5}	V_{IH} = V_{CC} ± 0.3 V; V_{IL} = V_{SS} ± 0.3 V			1	20	mA
V_{CC} Active Read-While-Program Current (1,2)	I_{CC6}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Word		85	180	mA
V_{CC} Active Program-While-Erase Current (1,2)	I_{CC7}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Word		85	180	mA
V_{CC} Active Program-While-Erase-Suspended Current (2,5)	I_{CC8}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			70	140	mA
Acc Accelerated Program Current	I_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Acc Pin		20	40	mA
			Vcc Pin		60	120	
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA, V_{CC} = 3.0				0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{CC} = 3.0			0.85 x Vcc		V
Low V_{CC} Lock-Out Voltage (4)	V_{LKO}			2.3		2.5	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V
4. Guaranteed by design, but not tested.

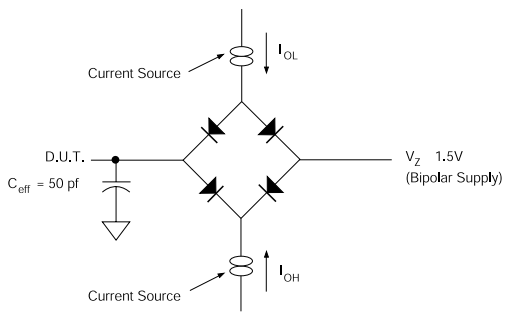
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	70		100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	35		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	30		30		30		30		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300		300	µs
Sector Erase Time	t_{WHWH2}			15		15		15		15	sec
Read Recovery Time (2)	t_{GHEL}		0		0		0		0		µs
Chip Programming Time				50		50		50		50	sec

1. Typical value for t_{WHWH1} is 9µs.
2. Guaranteed by design, but not tested.

FIG 2: AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-70		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		100		120		150		ns
Chip Select Setup Time	tELWL	tCS	0		0		0		0		ns
Write Enable Pulse Width	tWLWH	tWP	35		50		50		65		ns
Address Setup Time	tAVWL	tAS	0		0		0		0		ns
Data Setup Time	tDVWH	tDS	45		50		50		65		ns
Data Hold Time	tWHDX	tDH	0		0		0		0		ns
Address Hold Time	tWLAX	tAH	45		50		50		65		ns
Write Enable Pulse Width High	tWHWL	tWPH	30		30		30		35		ns
Duration of Byte Programming Operation (1)	tWHWH1			300	300		300			300	µs
Sector Erase	tWHWH2			15	15		15			15	sec
Read Recovery Time before Write (3)	tGHWL		0		0		0		0		µs
VCC Setup Time	tVCS		50		50		50		50		µs
Chip Programming Time				50		50		50		50	sec
Output Enable Setup Time		tOES	0		0		0		0		ns
Output Enable Hold Time (2)		tOEH	10		10		10		10		ns
Address Setup Time to $\overline{OE}$ low during toggle bit polling		tASO	15		15		15		15		ns
Address Hold Time From $\overline{CS}$ or $\overline{OE}$ high during toggle		tAHT	0		0		0		0		ns
Output Enable High during toggle bit polling		tOEPH	20		20		20		20		ns
Latency Between Read and Write Operations		tsr/W	0		0		0		0		ns
Write Recovery Time from RY/$\overline{BY}$		tRB	0		0		0		0		ns
Program/Erase Valis to RY/$\overline{BY}$		tBUSY	90		90		90		90		ns

1. Typical value for t_{WHWH1} is 9µs.
2. For Toggle and Data Polling.
3. Guaranteed by design, but not tested.

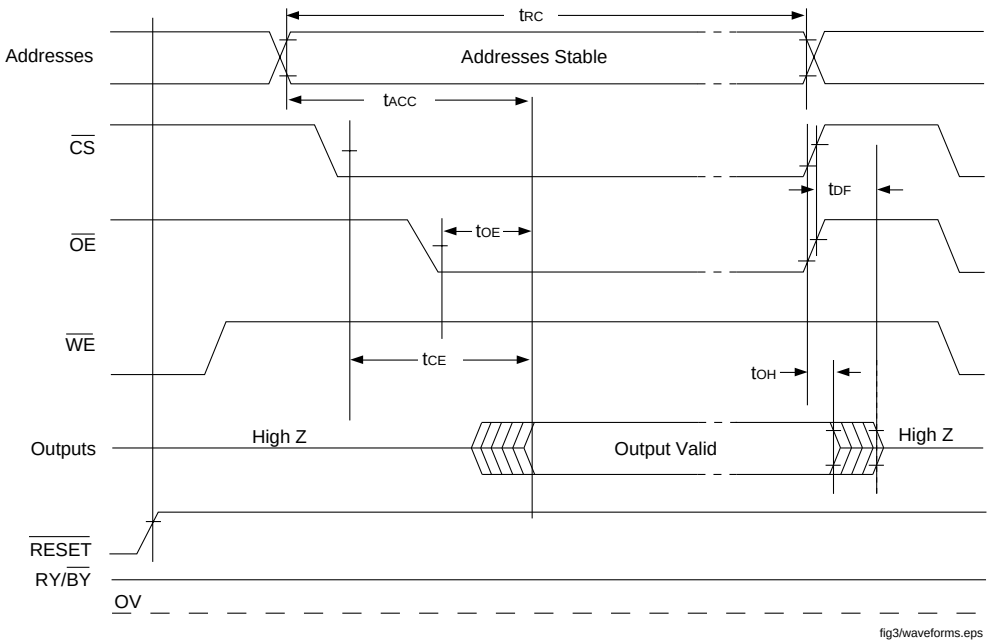
AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter		Symbol		-70		-100		-120		-150		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time		tAVAV	tRC	70		100		120		150		ns
Address Access Time		tAVQV	tACC		70		100		120		150	ns
Chip Select Access Time		tELQV	tCE		70		100		120		150	ns
Output Enable to Output Valid		tGLQV	tOE		40		40		50		55	ns
Chip Select High to Output High Z (1)		tEHQZ	tDF		30		30		30		40	ns
Output Enable High to Output High Z (1)		tGHQZ	tDF		30		30		30		40	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, Whichever is first		tAXQX	tOH	0			0		0			ns
Output Enable Hold Time (1)	Read		tOEH	0		0		0		0		
	Toggle and Data Polling			10		10		10		10		

1. Guaranteed by design, not tested.

FIG 3: AC WAVEFORMS FOR READ OPERATIONS



AC CHARACTERISTICS – HARDWARE RESET ($\overline{RESET}$)

Parameter	Symbol		-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read Mode (See Note)	t_{ready}			20		20		20	µs
$\overline{RESET}$ Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	t_{ready}			500		500		500	ns
$\overline{RESET}$ Pulse Width	t_{RP}		500		500		500		ns
$\overline{RESET}$ High Time Before Read (See Note)	t_{RH}		50		50		50		ns
$\overline{RESET}$ Low to Standby Mode	t_{RPD}		20		20		20		µs
RY/$\overline{BY}$ Recovery Time	t_{RB}		0		0		0		ns

Note: Not 100% tested.

FIG 4: RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

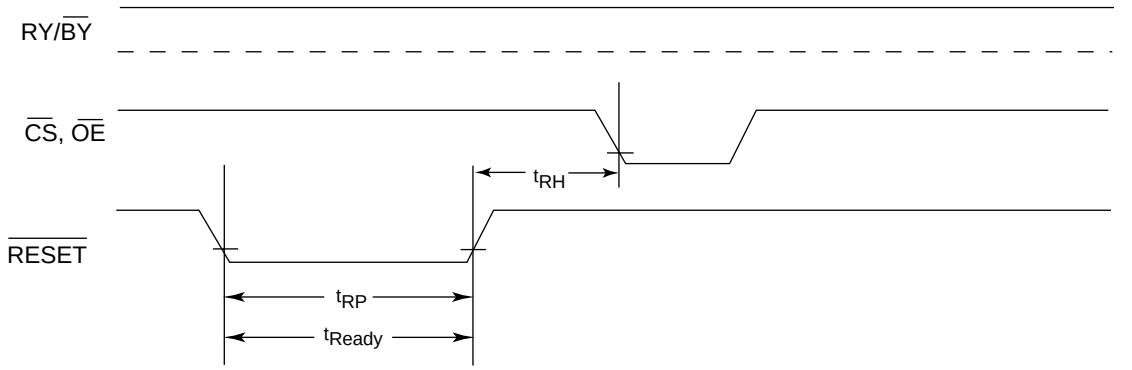


FIG 5: RESET TIMINGS DURING EMBEDDED ALGORITHMS

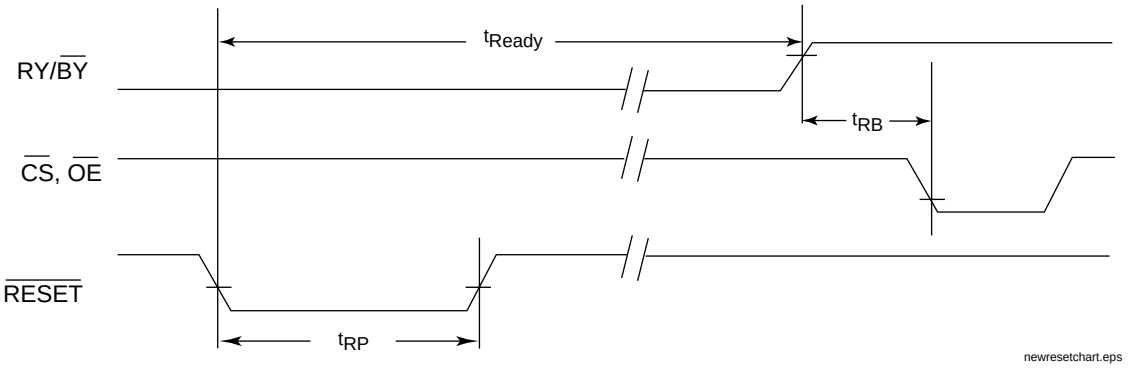
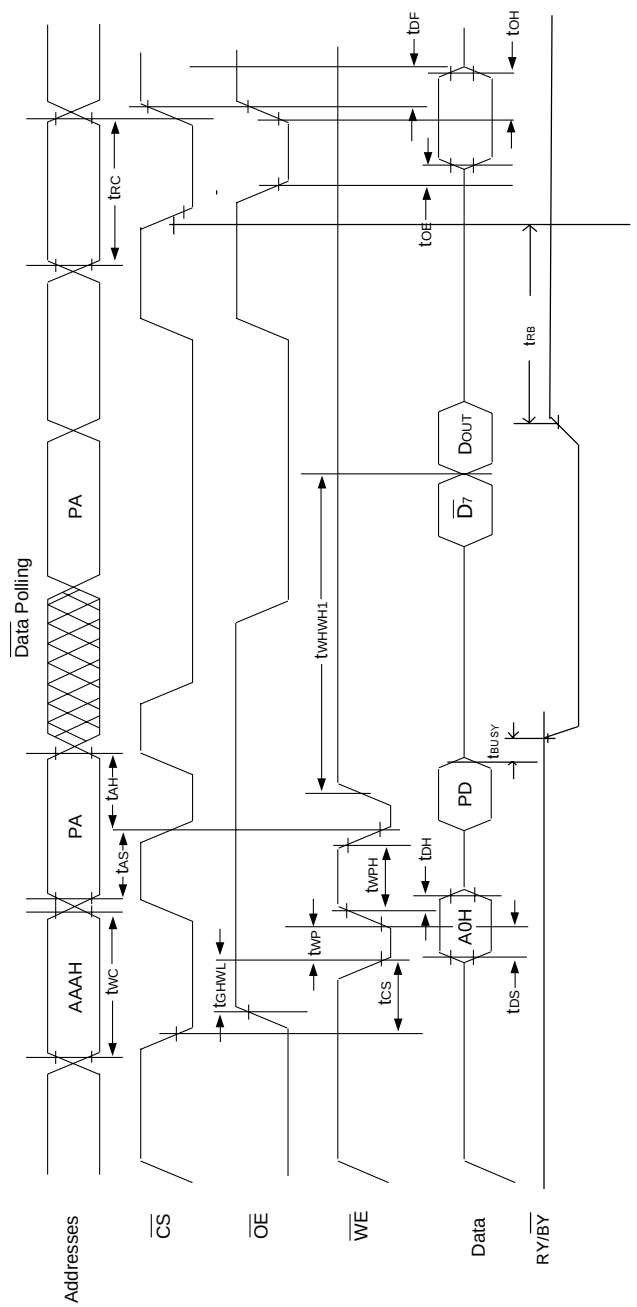


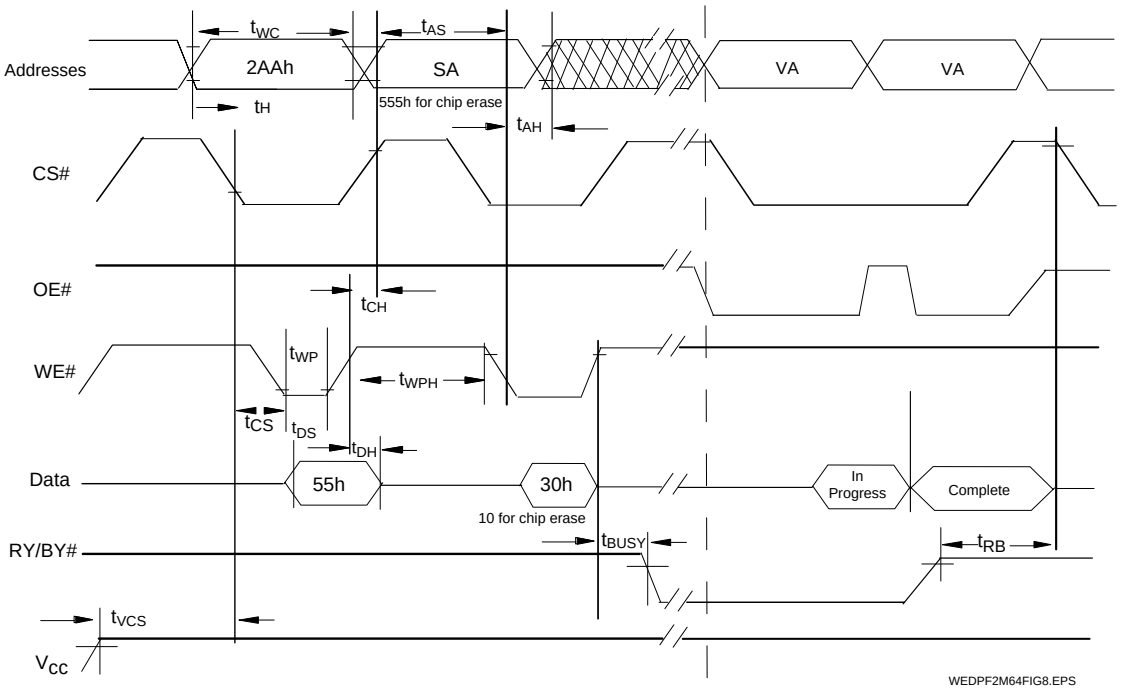
FIG 6: WRITE/ERASE/PROGRAM OPERATION, WE CONTROLLED



NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D_7}$ is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

FIG 7: ACCELERATED PROGRAM TIMING DIAGRAM

FIG 8: CHIP/SECTOR ERASE OPERATION TIMINGS



NOTES:
1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status").

FIG 9: BACK TO BACK READ/WRITE CYCLE TIMINGS

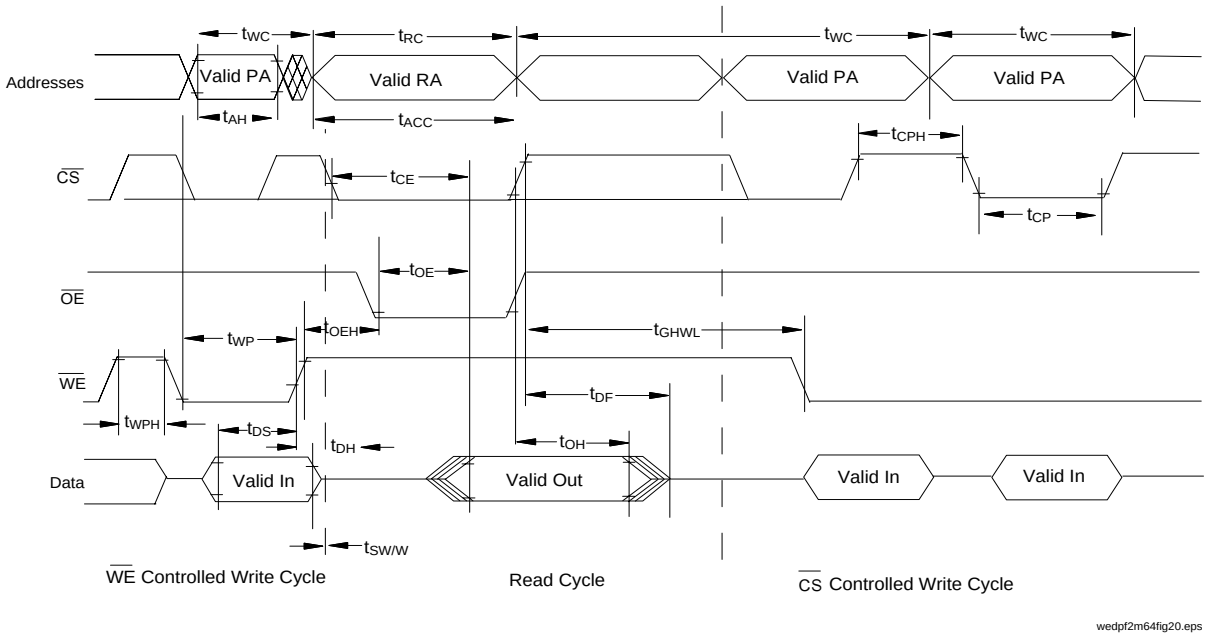
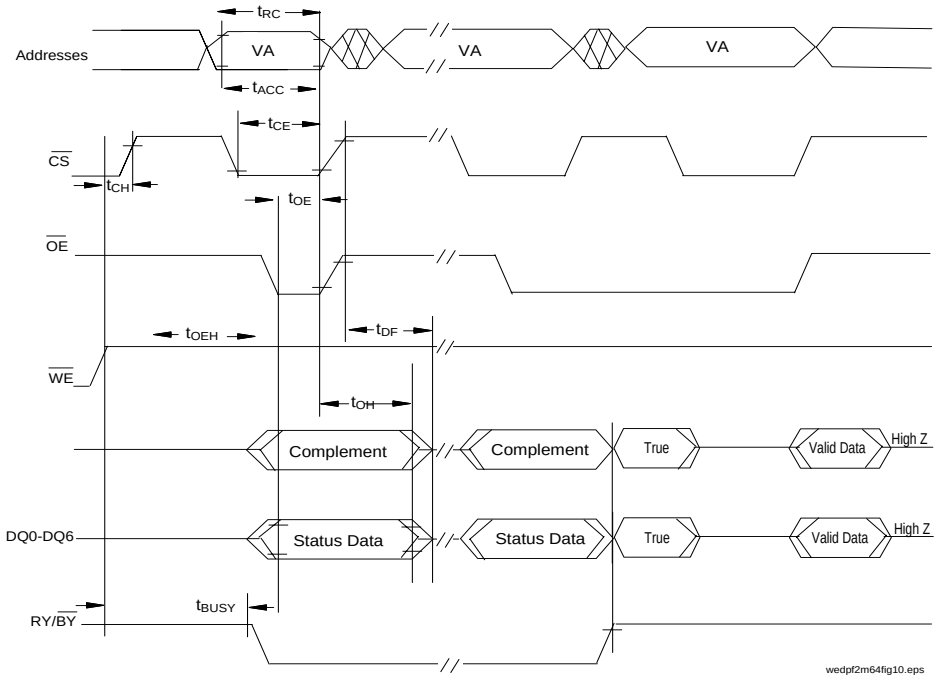
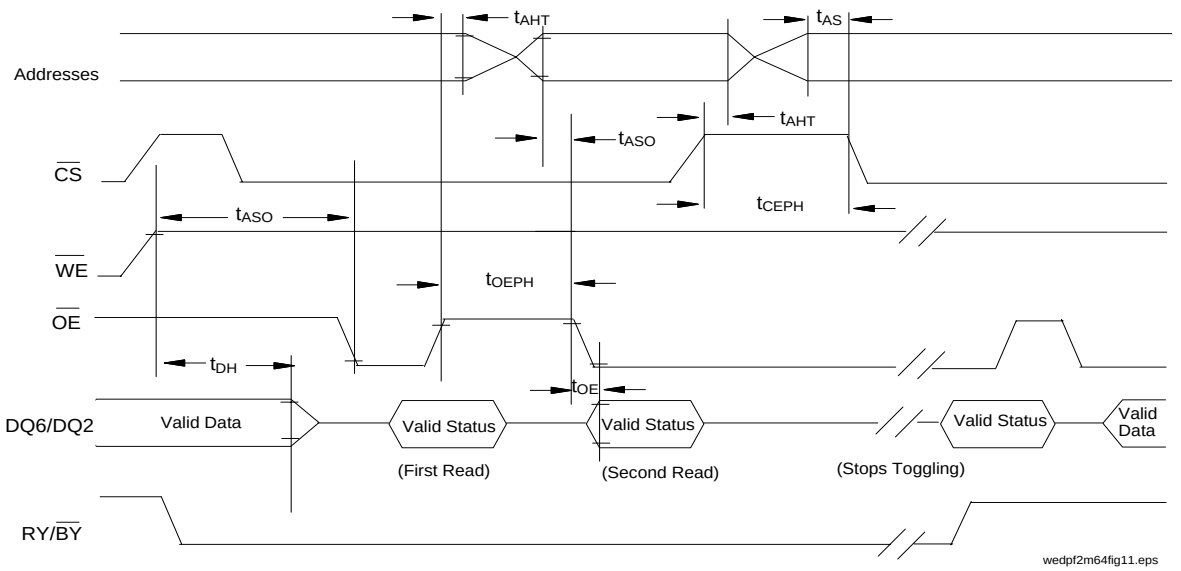


FIG. 10: DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



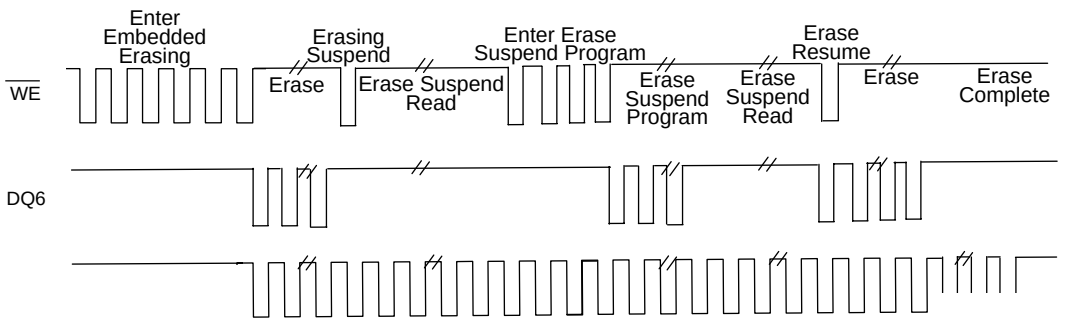
NOTE: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

FIG 11: TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



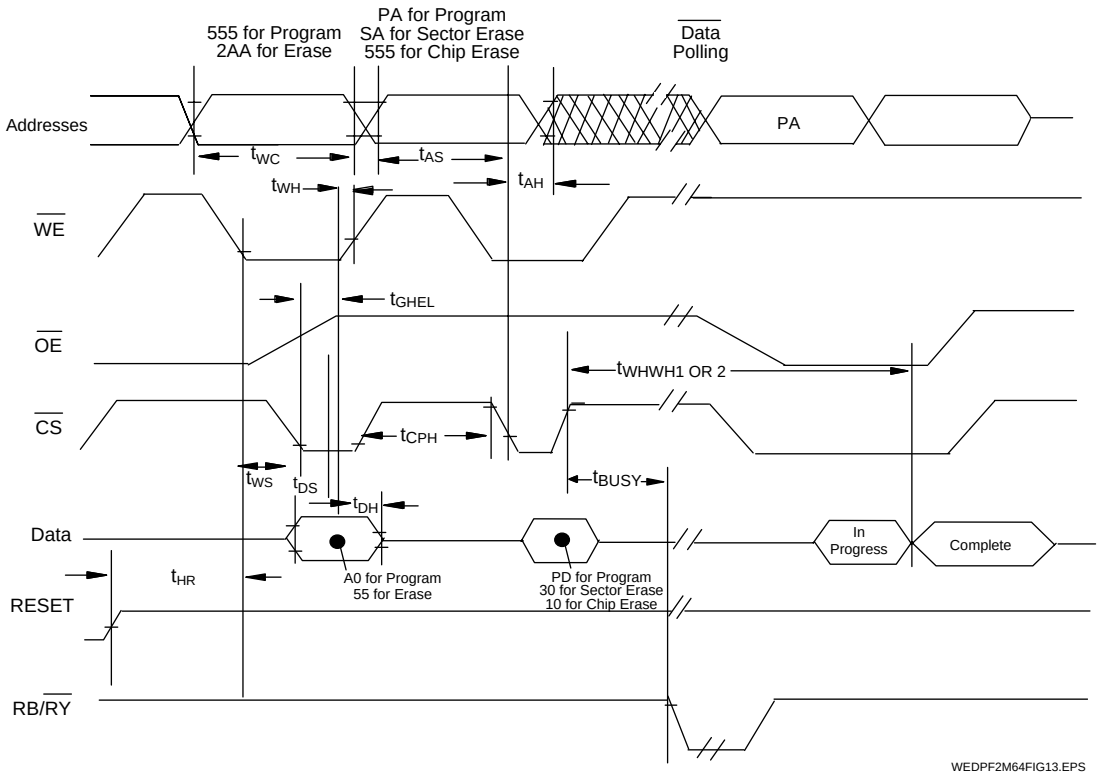
NOTE: VA = Valid address, not required for DQ6. Illustration shows first two status cycle after comand sequence, last status read cycle, and array data read cycle.

FIG 12: DQ2 VS. DQ6



NOTE: DQ2 toggles only when read at an address within an erase-suspended sector. The system may use $\overline{OE}$ or $\overline{CS}$.

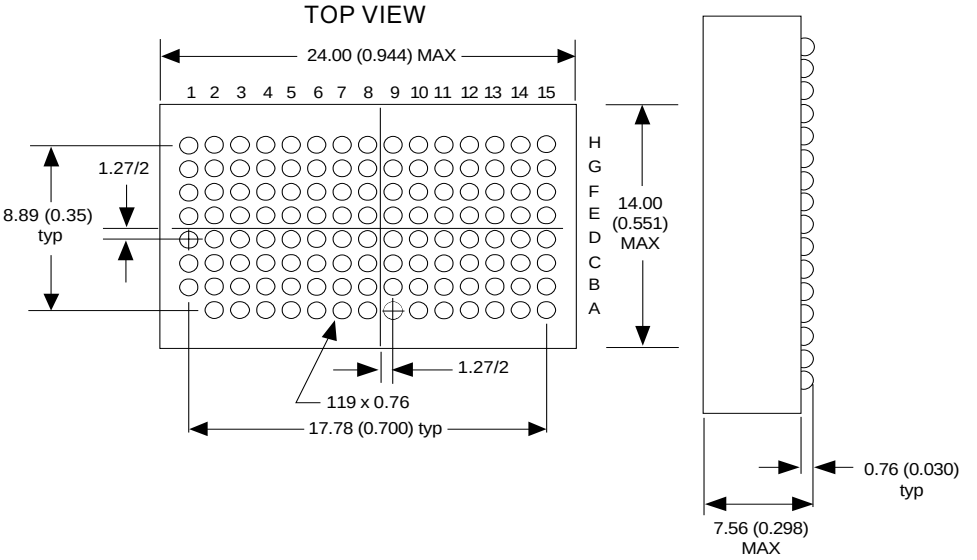
FIG 13: ALTERNATE $\overline{CS}$ CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS



NOTES:
1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. DQ7 is the complement of the data written to the device. D_{OUT} is the data written to the device.

PACKAGE: 119 STACKED TSOP BGA

TOP VIEW



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WED P F 2M64 B - XXX X B 3

PROGRAMMING VOLTAGE
3 = 3.3V

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

PACKAGE TYPE:
B = 119 Stacked TSOP BGA

ACCESS TIME (ns)

IMPROVEMENT MARK
B = Boot Block (Bottom Sector)

ORGANIZATION, 2M x 64
User configurable as 4M x 32, 8M x 16 or 16M x 8

Flash

Plastic

WHITE ELECTRONIC DESIGNS CORP.