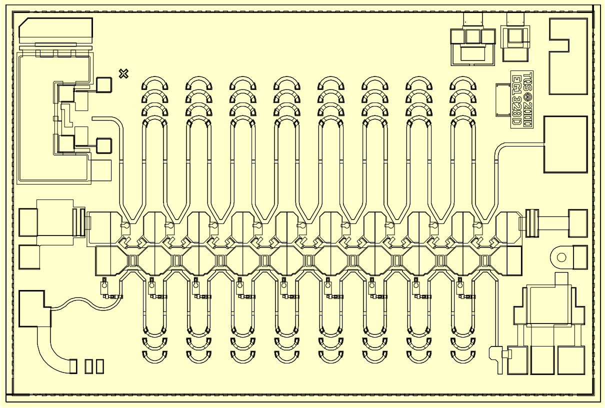
TriQuint SEMICONDUCTOR

Advance Product Datasheet

July 30, 2001

DC-18GHz MPA with AGC TGA1328-EPU

OC-192 12.5GB/s LN/MZ Driver and Receive AGC Applications



Description

The TriQuint TGA1328EPU is a medium power wideband AGC amplifier that typically provides 17dB midband gain with 17dB AGC range. Typical input and output return loss is <10dB. Typical Noise Figure is 2.5dB at 3GHz. Typical saturated output power is 24dBm in high bias and 18dBm at low bias. Small signal 3dB BW is 14GHz with saturated power performance to 18GHz. RF ports are DC coupled enabling the user to customize system corner frequencies. Applications include OC192 12.5GBit/s receive AGC amplifier and 4-8Vpp transmit LN/MZ driver amplifier.

Drain bias may be applied thru the on-chip drain termination resistor for low drive applications or thru the RF output port for high drive applications. A cascaded pair demonstrated greater than 8Vpp output voltage swing with less than 500mVpp at the input when stimulated with 10GBit/s. 2^31-1prbs. NRZ data.

The TGA1328 requires off-chip decoupling and blocking components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in chip form and will soon be available in a surface mount package.

Key Features and Performance

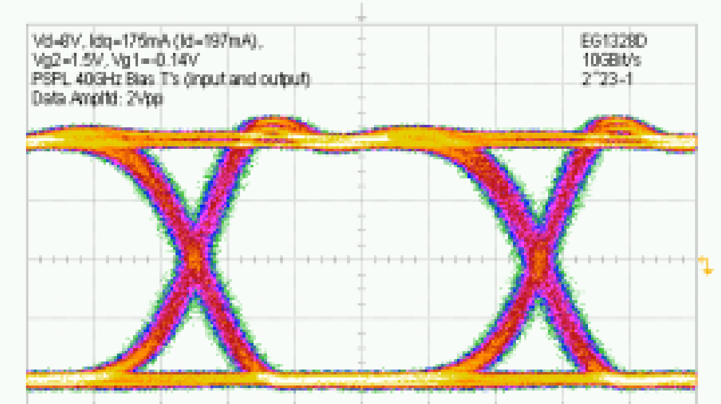
- 0.5um pHEMT Dual Gate Technology
- DC - 14GHz (small signal 3dB BW)
- DC-18GHz Saturated Power BW
- 17dB Gain / AGC Range
- Transmit or Receive OC-192 Application
- 8Vpp Electrical Eye (at power bias)
- Low Additive Jitter
- Power Bias: Vd = 8V @ 175 mA
- Low Noise Bias: V+ = 8V @ 80 mA
- Chip Dimensions 3.4mm x 2.3mm

Primary Applications

- 12.5GBit OC192 LN/MZ Driver
- 12.5GBit OC192 AGC Receive

Measured Performance

10GBit/s Performance
Output = 8V P-P, Input = 2V P-P
scale 2V/div, 20ps/div



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

MAXIMUM RATINGS

SYMBOL	PARAMETER 5/	VALUE	NOTES
V^+	POSITIVE SUPPLY VOLTAGE	10 V	
I^+	POSITIVE SUPPLY CURRENT	250 mA	1/
P_{IN}	INPUT CONTINUOUS WAVE POWER	23 dBm	4/
P_D	POWER DISSIPATION	2.6 W	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 ^{0}C	2/ 3/
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 ^{0}C	
T_{STG}	STORAGE TEMPERATURE	-65 to 150 ^{0}C	

1/ Total current .

2/ These ratings apply to each individual FET.

3/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

4/ This value reflects an estimate. Actual value will be inserted as soon as it is determined.

5/ These ratings represent the maximum operable values for the device.

DC SPECIFICATIONS (100%)
(T_A = 25 °C ± 5 °C)

COMPONENT	PARAMETER	CONDITIONS	UNITS	MIN	MAX
Q1-9DG	IDSS	STD	mA	220	516
Q1-9DG	GM	STD	mS	241	581
Q1-9DG	BVGS	STD	V	-30	-15
Q1-9DG	BVGD	STD	V	-30	-15
Q1-9DG	VP1	STD	V	-1.5	-.5
Q1-9DG	VP2	STD	V	-1.5	-.5

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RF SPECIFICATIONS

(T_A = 25°C ± 5°C)

NOTE	TEST	MEASUREMENT CONDITIONS 8V @ 175mA	VALUE			UNITS
			MIN	TYP	MAX	
	3dB BANDWIDTH			14		GHz
	SATURATED POWER BW			18		GHz
1/	SMALL-SIGNAL GAIN MAGNITUDE	Midband		17		dB
	SMALL SIGNAL AGC RANGE	Midband		17		dB
	NOISE FIGURE	3GHz		2.5		dB
	SATURATED OUTPUT VOLTAGE	DC-18GHz		8		V
	SATURATED OUTPUT POWER	DC-18GHz		24		dBm
1/	INPUT RETURN LOSS MAGNITUDE	DC-18GHz		-12		dB
1/	OUTPUT RETURN LOSS MAGNITUDE	DC-18GHz		-12		dB
	ADDITIVE JITTER			< 2		pS
	GROUP DELAY	DC-14GHz		+/- 20		pS
	RISE TIME			< 30		pS

Notes:

1/ Measured at RF probe

THERMAL INFORMATION*

Parameter	**Test Condition**	**T_{CH} (°C)**	**$R_{\theta JC}$ (°C/W)**	**T_M (HRS)**
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	V+ = 8 V, V_{ctrl} = 1.5 V, I_D = 80 mA ±5%	88.50	28.91	4.4E+8

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

* The thermal information is a result of a detailed thermal model.

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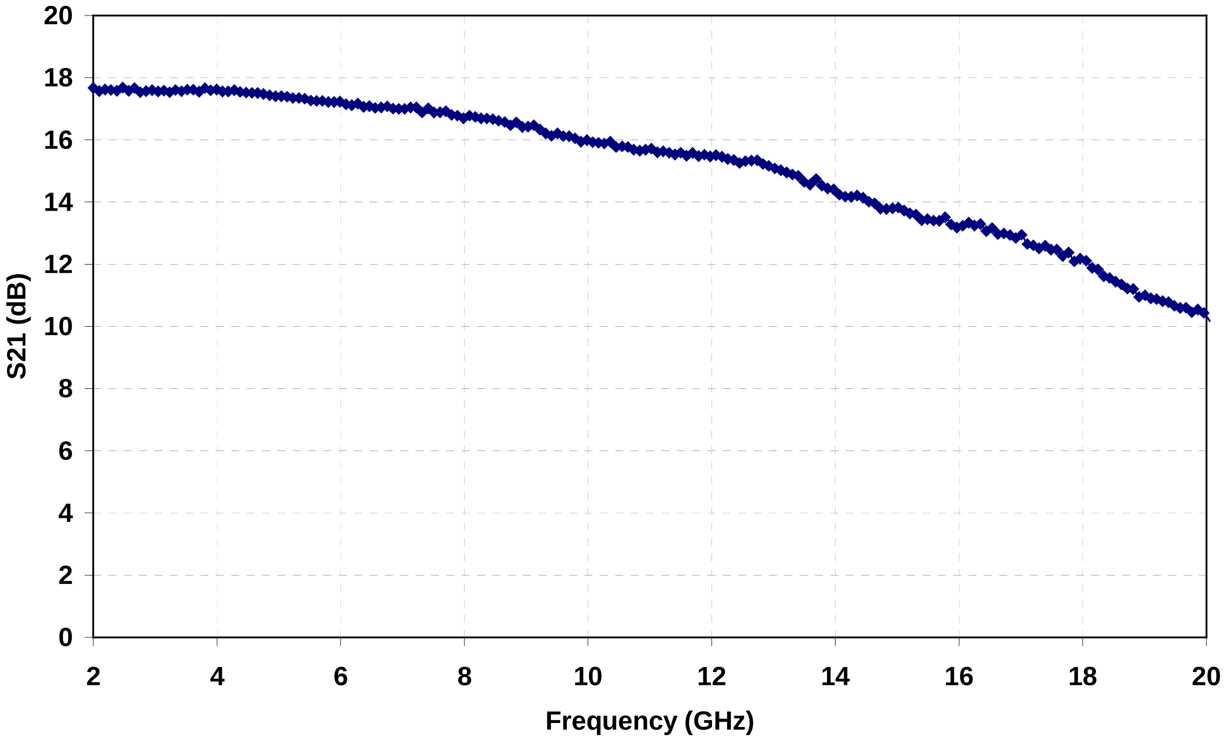
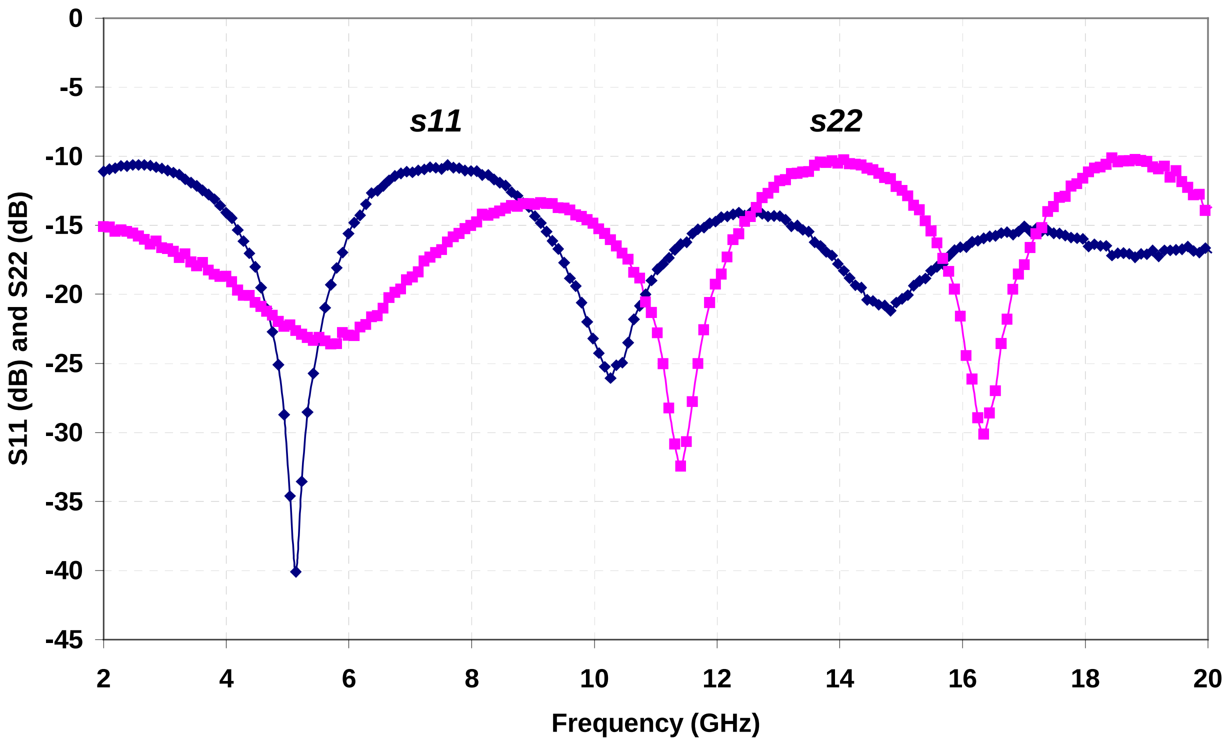
TGA1328 Typical Measured S-parameters





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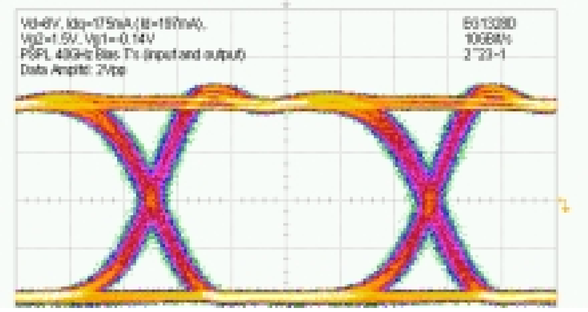
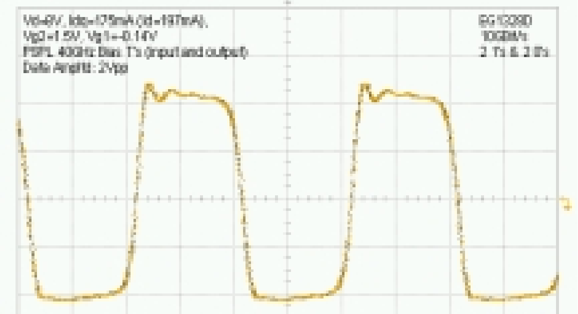
Measured Performance

8V P-P (Saturated)

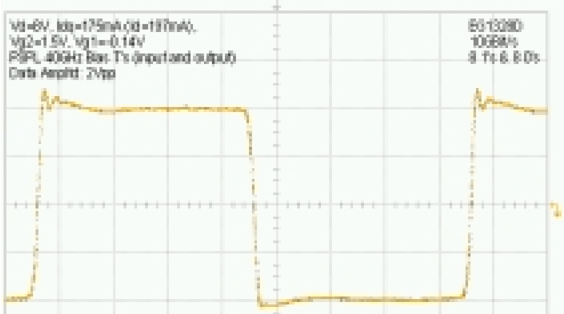


10GBit/s Performance
Output = 8V P-P, Input = 2V P-P
scale 2V/div, 20ps/div

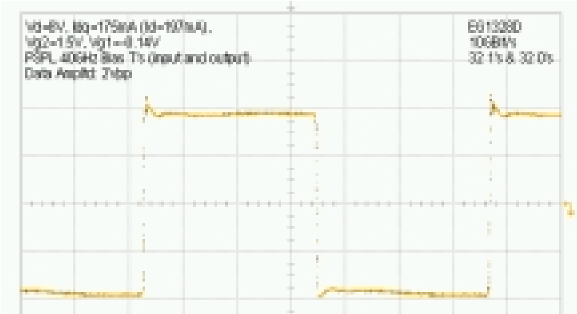
8V P-P



2 1’s and 2 0’s, 100ps/div

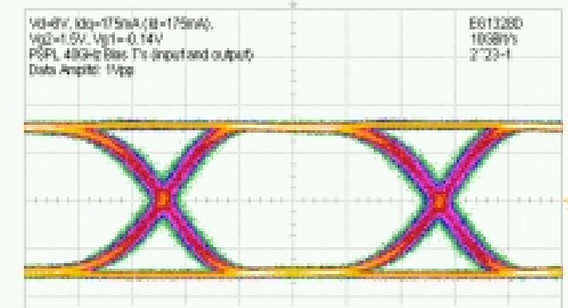


8 1’s and 8 0’s, 200ps/div



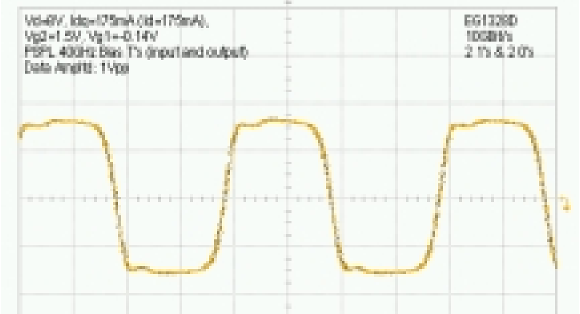
32 1’s and 32 0’s, 1ns/div

6V P-P (Near Small Signal)

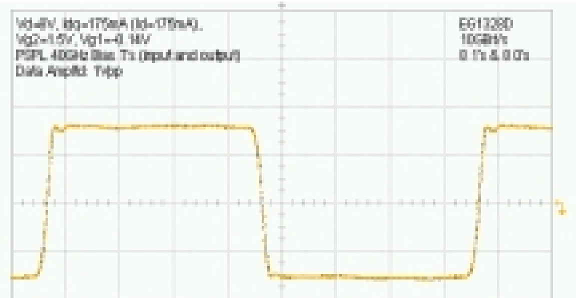


10GBit/s Performance
Output =6V P-P, Input = 1V P-P
scale 2V/div, 20ps/div

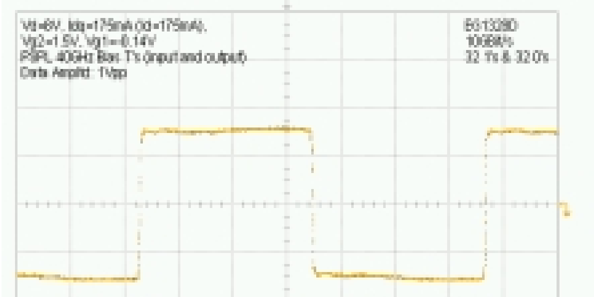
6V P-P



2 1’s and 2 0’s, 100ps/div



8 1’s and 8 0’s, 200ps/div



32 1’s and 32 0’s, 1ns/div

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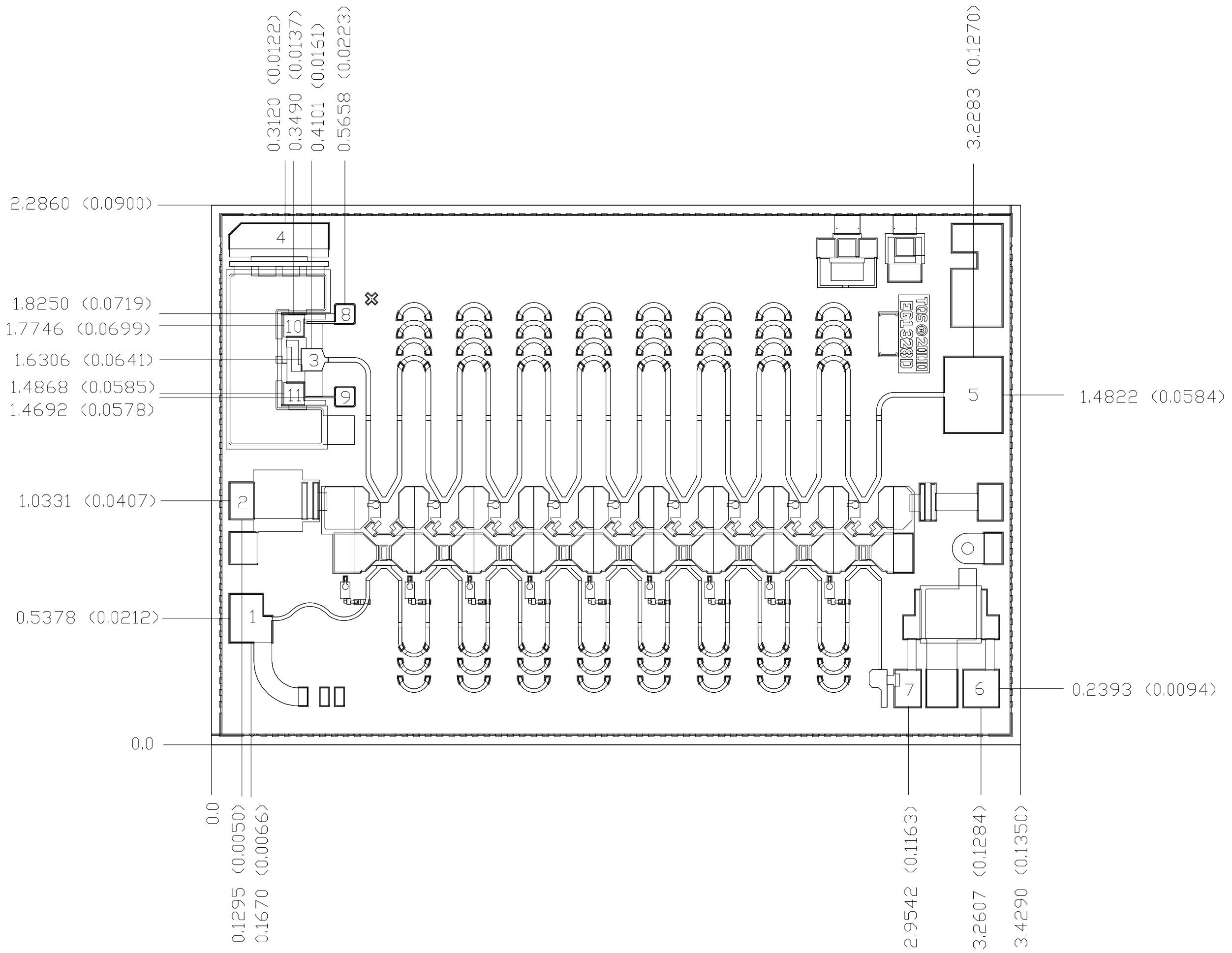

Units: millimeters (inches)
Thickness: 0.1016 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.0508 (0.002)

Bond Pad #1 (RF Input)	0.152 x 0.203 (0.006 x 0.008)
Bond Pad #2 (Vctrl)	0.102 x 0.152 (0.004 x 0.006)
Bond Pad #3 (Vd)	0.076 x 0.152 (0.003 x 0.006)
Bond Pad #4 (V+)	0.419 x 0.152 (0.016 x 0.006)
Bond Pad #5 (RF Output)	0.254 x 0.330 (0.010 x 0.0013)
Bond Pad #6 (V-)	0.152 x 0.152 (0.006 x 0.006)
Bond Pad #7 (Vaux)	0.127 x 0.152 (0.005 x 0.006)
Bond Pad #8 (resistor tune)	0.085 x 0.085 (0.003 x 0.003)
Bond Pad #9 (resistor tune)	0.085 x 0.085 (0.003 x 0.003)
Bond Pad #10 (resistor tune)	0.091 x 0.095 (0.0036 x 0.0037)
Bond Pad #11 (resistor tune)	0.091 x 0.095 (0.0036 x 0.0037)

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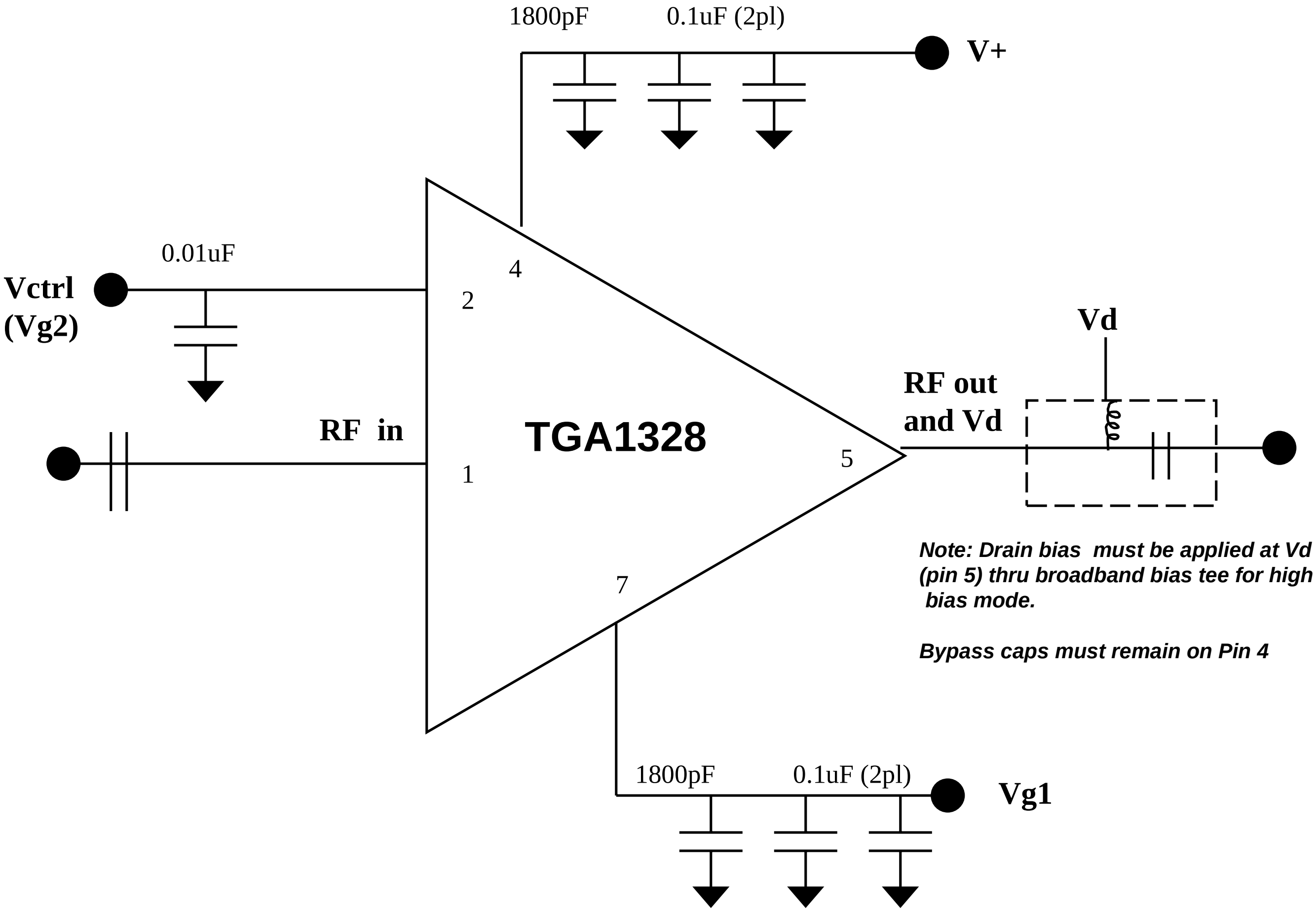

Note: Drain bias must be applied at Vd (pin 5) thru broadband bias tee for high bias mode.

Bypass caps must remain on Pin 4

Bias Procedure

1) Make sure no RF power is applied to the device before continuing.

2) Pinch off device by setting V_{G1} to –2.5V.

3) Raise V_D to 8.0V while monitoring drain current. Current should be zero.

NOTE: ***V_D bias should be applied to the RF output port via a bias tee for high power bias***.

4) Raise V_{G2} to 1.5V (no greater than 1.5V).

5) Make V_{G1} more positive until drain current reaches 175mA. (80 mA for low noise bias)

6) Apply RF power.

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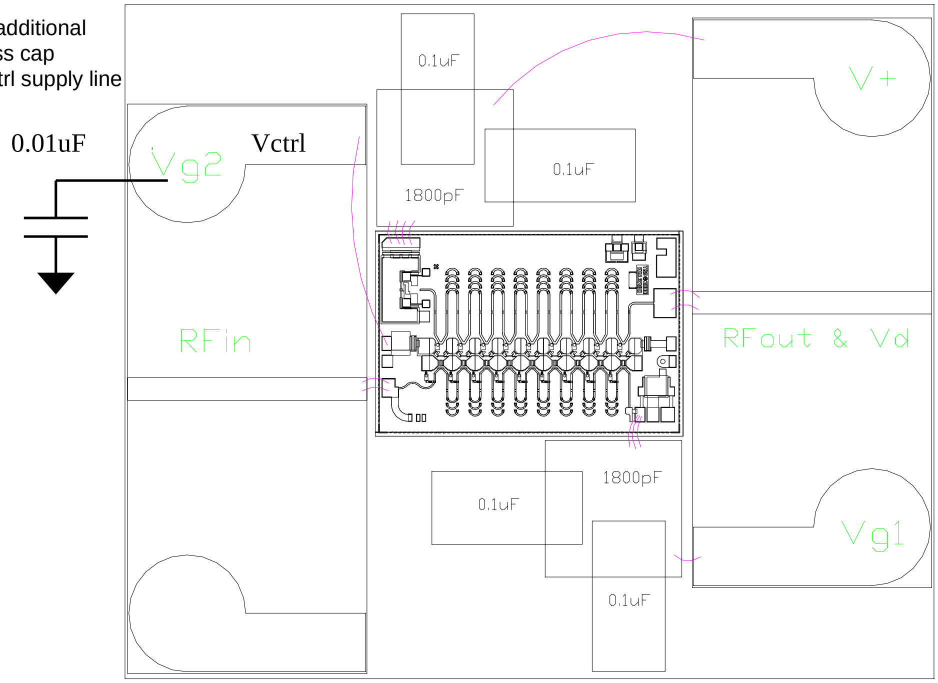

Recommend additional
0.01uF bypass cap
located on Vctrl supply line
on test fixture

Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200 °C

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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