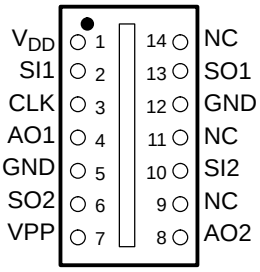
- **256 × 1 Sensor-Element Organization**
- **400 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Low Noise for 256 Gray-Scale Applications**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 2 MHz**
- **Single 5-V Supply**

(TOP VIEW)



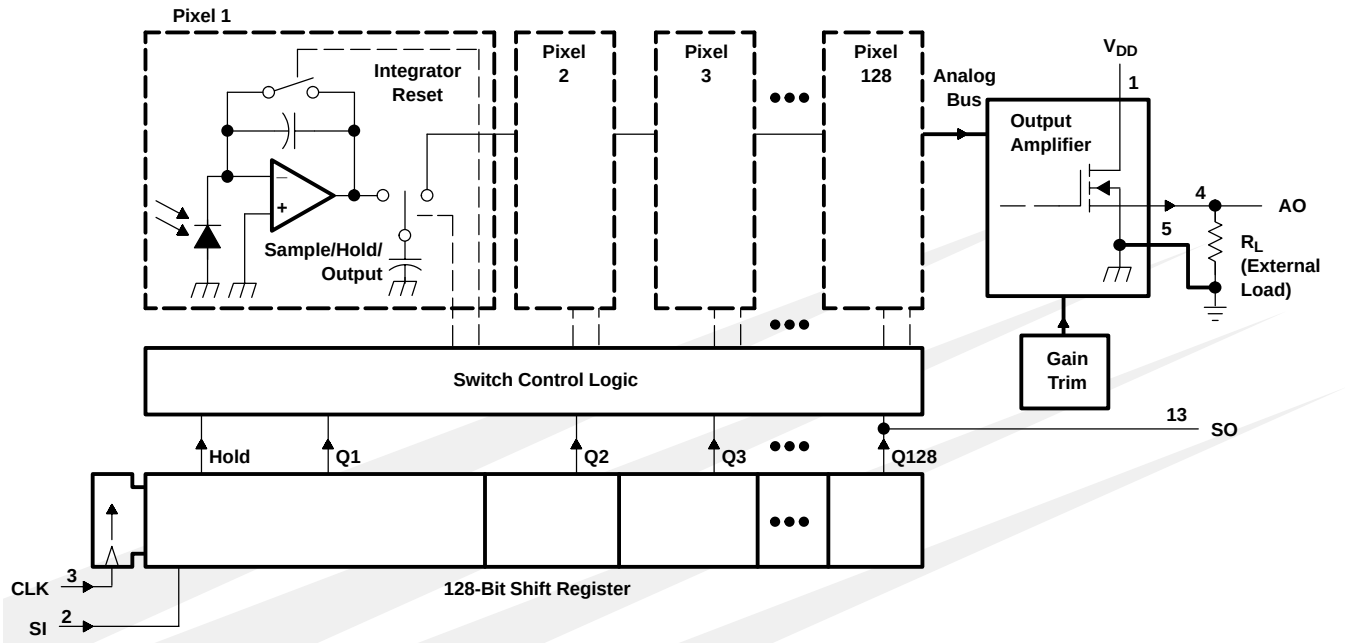
NC – No internal connection

Description

The TSL1402 linear sensor array consists of two sections of 128 photodiodes each and associated charge amplifier circuitry, aligned to form a contiguous 256 × 1 pixel array. The device incorporates a pixel data-hold function that provides simultaneous integration start and stop times for all pixels. The pixels measure 63.5 µm by 55.5 µm, with 63.5-µm center-to-center spacing and 8-µm spacing between pixels. Operation is simplified by internal logic requiring only a serial-input pulse (SI) and a clock.

The TSL1402 is intended for use in a wide variety of applications including mark and code reading, OCR and contact imaging, edge detection and positioning, and optical encoding.

Functional Block Diagram (each section – pin numbers apply to section 1)



Texas Advanced Optoelectronic Solutions Inc.
800 Jupiter Road, Suite 205 • Plano, TX 75074 • (972) 673-0759

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO1	4	Analog output of section 1
AO2	8	Analog output of section 2
CLK	3	Clock. Clk controls charge transfer, pixel output, and reset.
GND	5,12	Ground (substrate). All voltages are referenced to GND.
NC	9, 11, 14	No internal connection
SI1	2	Serial input (section 1). SI1 defines the start of the data-out sequence for section 1.
SI2	10	Serial input (section 2). SI2 defines the start of the data-out sequence for section 2.
SO1	13	Serial output (section 1). SO1 provides a signal to drive the SI2 input (in serial connection).
SO2	6	Serial output (section 2). SO2 provides a signal to drive the SI input of another device for cascading or as an end-of-data indication.
V_{DD}	1	Supply voltage. Supply voltage for both analog and digital circuitry.
VPP	7	Connected to GND

Detailed Description

Device operation (assumes serial connection)

The sensor consists of 256 photodiodes, called pixels, arranged in a linear array. Light energy impinging on a pixel generates photocurrent, which is then integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity on that pixel and the integration time.

The output and reset of the integrators is controlled by a 256-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI1. An internal signal, called Hold, is generated from the rising edge of SI1 and simultaneously transmitted to sections 1 and 2. This causes all 256 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. Simultaneously, during the first 18 clock cycles, all pixel integrators are reset, and the next integration cycle begins on the 19th clock. On the 128th clock rising edge, the SI pulse is clocked out on the SO1 pin (section 1) and becomes the SI pulse for section 2 (SI2). The rising edge of the 129th clock cycle terminates the SO1 pulse, and returns the analog output AO1 of section 1 to high-impedance state. Analog output AO2 now becomes the active output. As in section 2, SO2 is clocked out on the 256th clock pulse. Note that a 257th clock pulse is needed to terminate the SO2 pulse and return AO2 to the high-impedance state.

AO is driven by a source follower that requires an external pulldown resistor. When AO is not in the output phase, it is in a high-impedance state. The output is nominally 0 V for no light input and 2 V for a nominal white level output, with a nominal full–scale (saturation) voltage of 3 V.

The TSL1402 can be connected in the serial mode, where it takes 256 clocks to read out all pixels, or in the parallel mode where it takes 128 clocks to read out all pixels (see application section).

Absolute Maximum Ratings†

Supply voltage, V_{DD} . . . . . 7 V
Digital output voltage range, V_O . . . . . –0.5 V to V_{DD} + 0.5 V
Digital output current range, I_O . . . . . –10 mA to 10 mA
Digital input current range, I_I . . . . . –20 mA to 20 mA
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
Input voltage, V_I		0		V_{DD}	V
High-level input voltage, V_{IH}		$V_{DD} \times 0.7$		V_{DD}	V
Low-level input voltage, V_{IL}		0		$V_{DD} \times 0.3$	V
Wavelength of light source, λ		400		1000	nm
Clock frequency, f_{clock}		5		2000	kHz
Sensor integration time, t_{int}	Serial connection	0.1195	5	100	ms
	Parallel connection	0.0555	5	100	
Setup time, Serial input, $t_{su(SI)}$		20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 1)		0			ns
Operating free-air temperature, T_A		0		70	°C

NOTE 1: SI must go low before the rising edge of the next clock pulse.

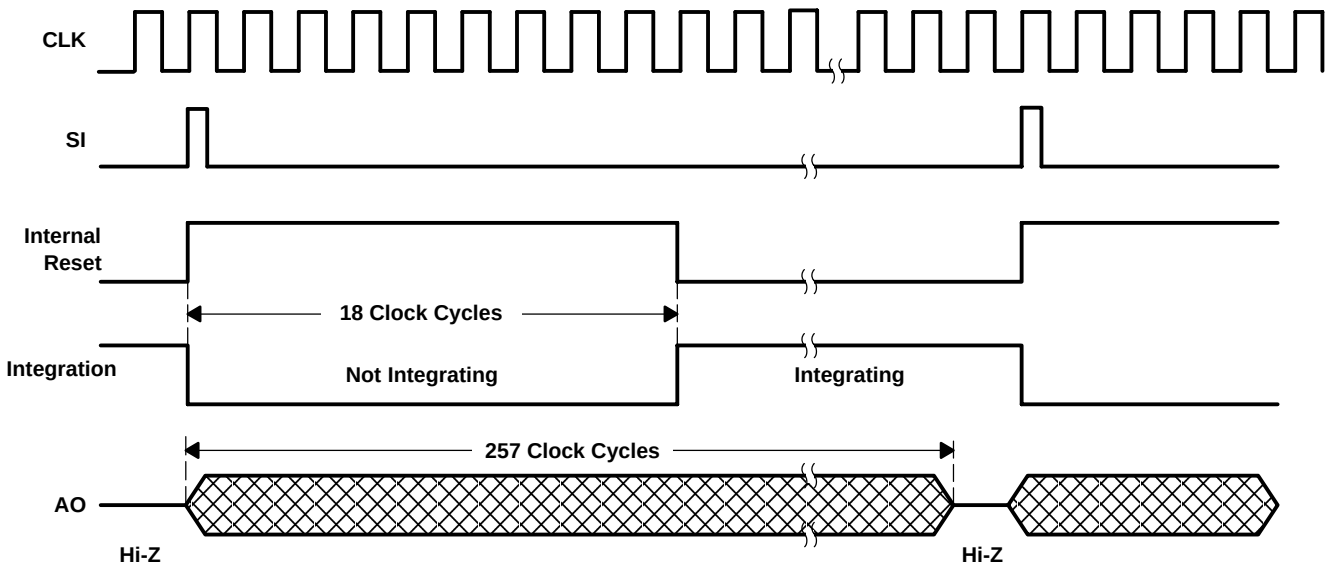


Figure 1. Timing Waveforms (Serial Connection)

Electrical Characteristics at f_{clock} = 200 kHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 565 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 14 μW/cm² (unless otherwise noted) (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Analog output voltage (white, average over 256 pixels)		1.6	2	2.4	V
	Analog output voltage (dark, average over 256 pixels)	E_e = 0	0	0.1	0.2	V
PRNU	Pixel response nonuniformity	See Note 3			±10%	
	Nonlinearity of analog output voltage	See Note 4		±0.4%		
	Output noise voltage	E_e = 0, See Note 5		1		mVrms
	Saturation exposure	See Note 6	95	123		nJ/cm²
	Analog output saturation voltage		3	3.5		V
DSNU	Dark signal nonuniformity	All pixels, E_e = 0, See Note 7		0.04	0.12	V
IL	Image lag	See Note 8		0.5%		
I_{DD}	Supply current	R_L = 330 Ω		5	8	mA
I_{IH}	High-level input current	$V_I = V_{DD}$			10	μA
I_{IL}	Low-level input current	V_I = 0			10	μA
C_i	Input capacitance			10		pF

NOTES: 2. Clock duty cycle is assumed to be 50%.

3. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated.
4. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
5. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
6. Minimum saturation exposure is calculated using the maximum responsivity and minimum output saturation voltage figures.
7. DNSU is the difference between the maximum and minimum of dark-current voltage.
8. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{AO} - V_{AO(dark)}}{V_{AO(white)} - V_{AO(dark)}} \times 100$$

Operating Characteristics over recommended ranges of supply voltage and operating free-air temperature unless otherwise noted (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(SO)}$	Propagation delay time, SO1, SO2			50		ns
t_w	Clock high or low		50			ns
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 50 pF		350		ns

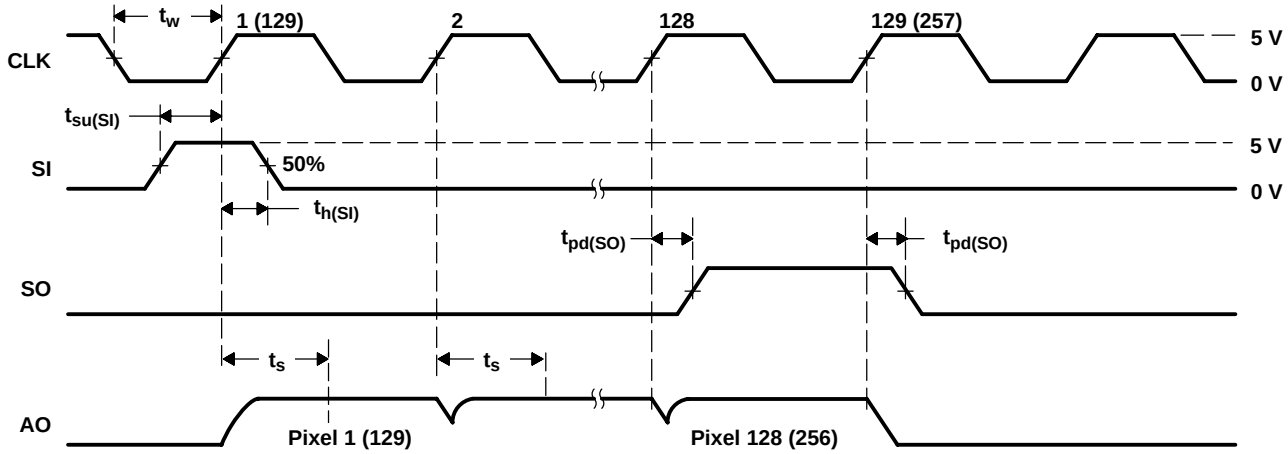


Figure 2. Operational Waveforms (each section)

APPLICATION INFORMATION

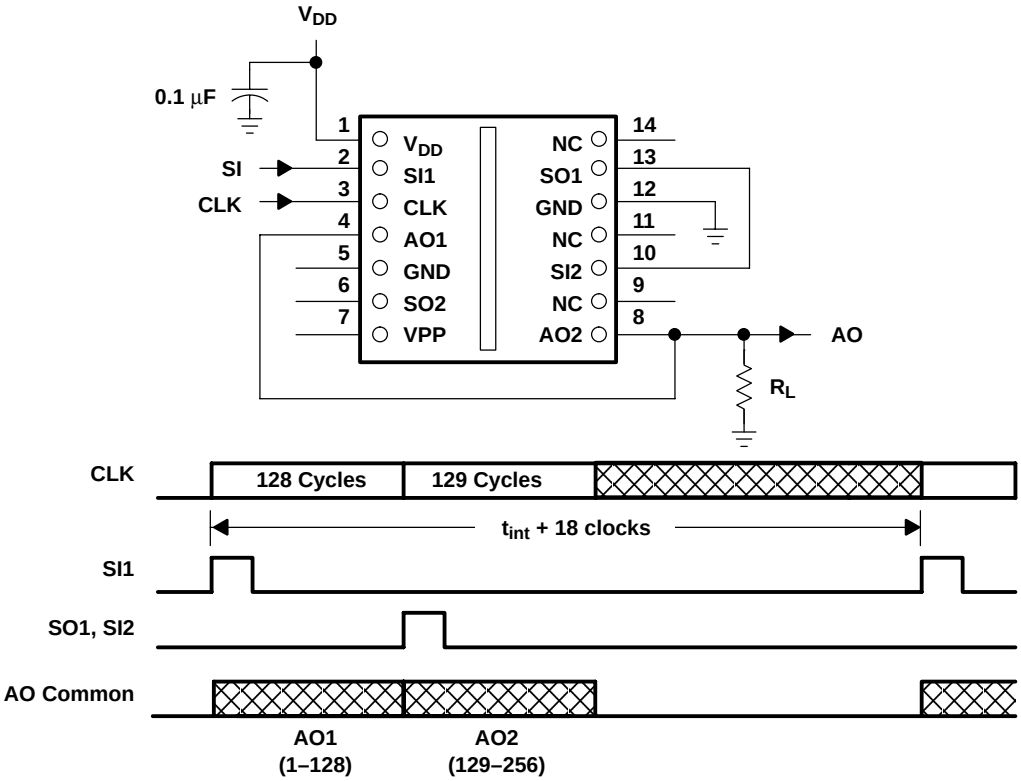


Figure 3. Serial Connection

APPLICATION INFORMATION

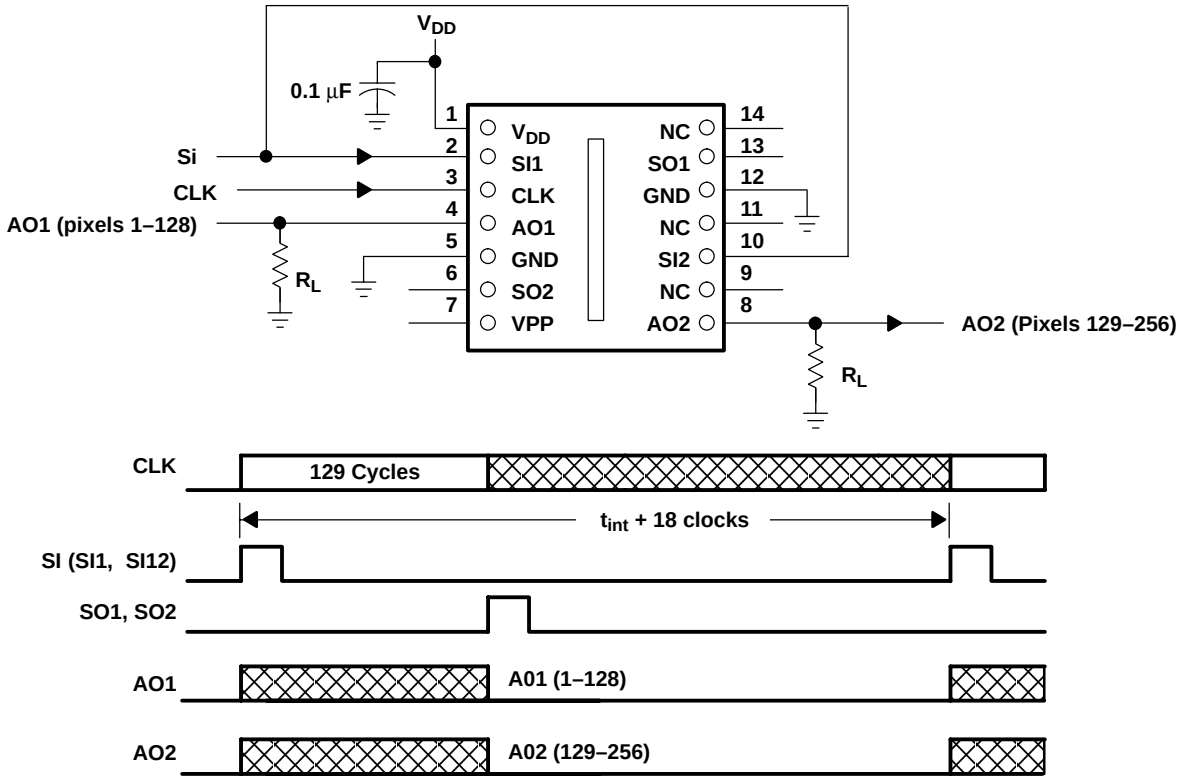


Figure 4. Parallel Connection

TYPICAL CHARACTERISTICS

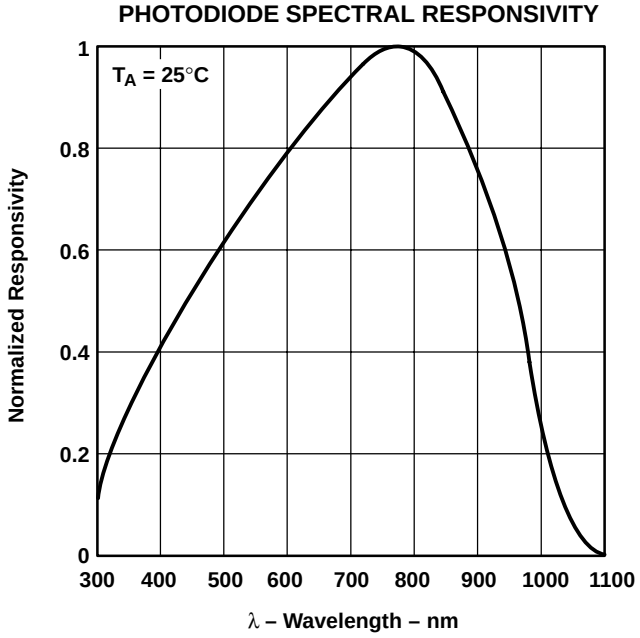
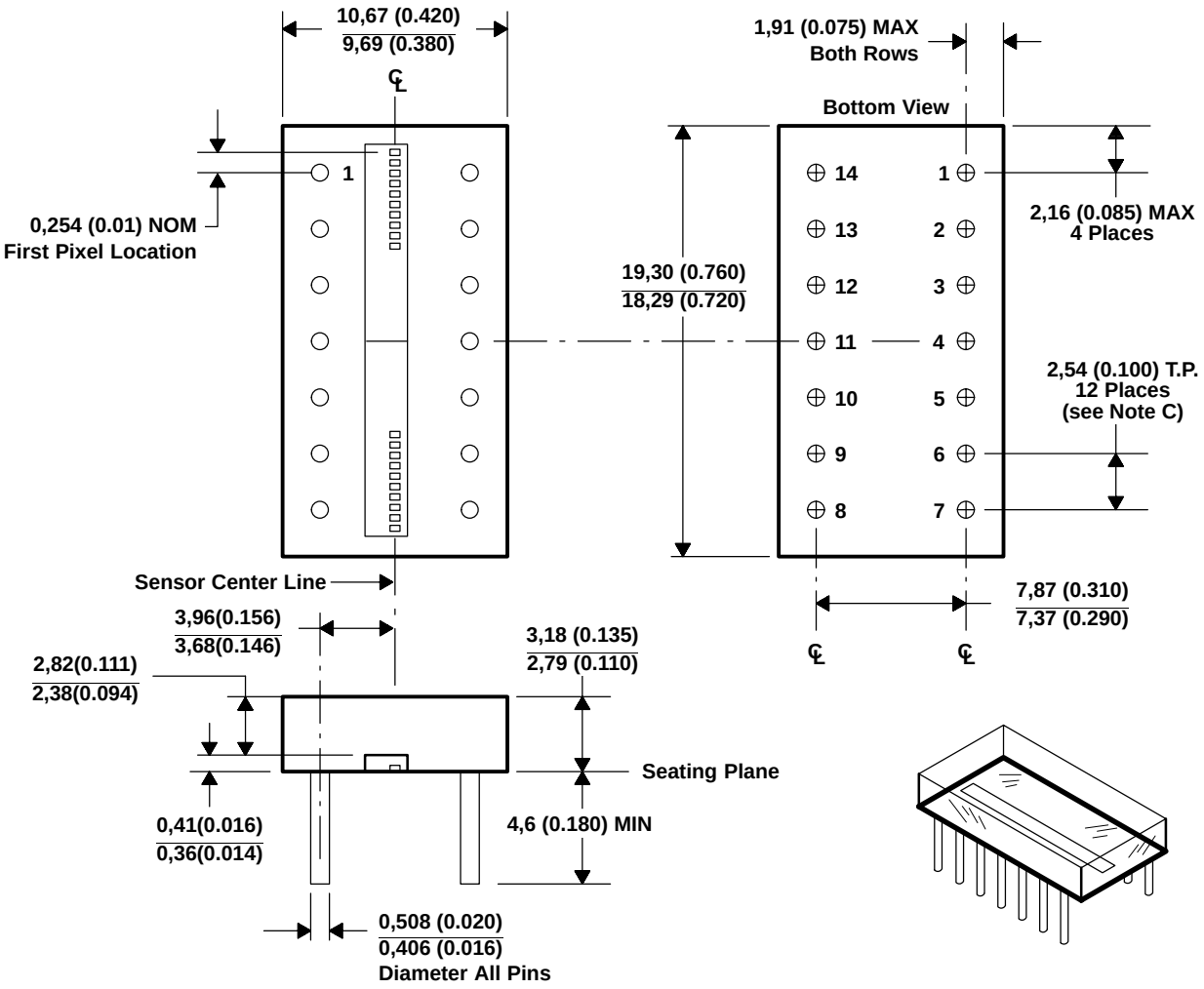


Figure 5

MECHANICAL INFORMATION

This assembly consists of a sensor chip mounted on a printed-circuit board in a clear molded plastic package. The distance between the top surface of the package and the surface of the sensor is nominally 1 mm (0.040 inch).



NOTES: D. All linear dimensions are in inches (millimeters).
E. This drawing is subject to change without notice.
F. The true-position spacing is 2,54 mm (0.100 inch) between lead centerlines. Each pin centerline is located within 0,25 mm (0.010 inch) of its true longitudinal positions.
G. Index of refraction of mold compound = 1.5
H. Designation per JEDEC Std. 30: PDIP-T14

Figure 6. Clear Molded Plastic Package

PRODUCTION DATA — information in this document is current at publication date. Products conform to specifications in accordance with the terms of Texas Advanced Optoelectronic Solutions, Inc. standard warranty. Production processing does not necessarily include testing of all parameters.

NOTICE

Texas Advanced Optoelectronic Solutions, Inc. (TAOS) reserves the right to make changes to the products contained in this document to improve performance or for any other purpose, or to discontinue them without notice. Customers are advised to contact TAOS to obtain the latest product information before placing orders or designing TAOS products into systems.

TAOS assumes no responsibility for the use of any products or circuits described in this document or customer product design, conveys no license, either expressed or implied, under any patent or other right, and makes no representation that the circuits are free of patent infringement. TAOS further makes no claim as to the suitability of its products for any particular purpose, nor does TAOS assume any liability arising out of the use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

TEXAS ADVANCED OPTOELECTRONIC SOLUTIONS, INC. PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN CRITICAL APPLICATIONS IN WHICH THE FAILURE OR MALFUNCTION OF THE TAOS PRODUCT MAY RESULT IN PERSONAL INJURY OR DEATH. USE OF TAOS PRODUCTS IN LIFE SUPPORT SYSTEMS IS EXPRESSLY UNAUTHORIZED AND ANY SUCH USE BY A CUSTOMER IS COMPLETELY AT THE CUSTOMER'S RISK.