SGS-THOMSON MICROELECTRONICS

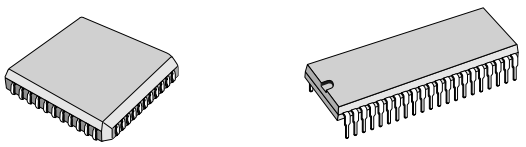
# L6285

## 3 CHANNELS MULTIPOWER SYSTEM

**ADVANCE DATA**

- CHANNEL-A AND CHANNEL-B FOR UNIPOLAR STEPPER MOTORS
  – LOW SIDE: $R_{DSON}$ = 1.2Ω
  – HIGH SIDE ; $R_{DSON}$ = 1.2Ω
- CHANNEL-C FOR DC MOTORS
  – LOW SIDE: $R_{DSON}$ = 1.7Ω
  – HIGH SIDE: $R_{DSON}$ = 1.2Ω
- CHOPPING MODE DRIVING FOR C.L. CURRENT CONTROL ON CHA AND CHB AND O.L. VOLTAGE CONTROL ON CHC.
- INTERNAL FOUR DRIVING LATCHES
- 16 BIT INTERNAL SHIFT REGISTER
- DIRECT INTERFACE TO µP
- SERIAL DRIVING SEQUENCE LOADING
- CMOS COMPATIBLE INPUTS
- PRE-ALARM OUTPUT SIGNAL
- THERMAL SHUTDOWN

**MULTIPOWER BCD TECHNOLOGY**



**PLCC44** **SDIP42**

**ORDERING NUMBERS:**
L6285 L6285S

### DESCRIPTION

This Combo Motor Driver uses large scale integration to incorporate several functions into the same chip.

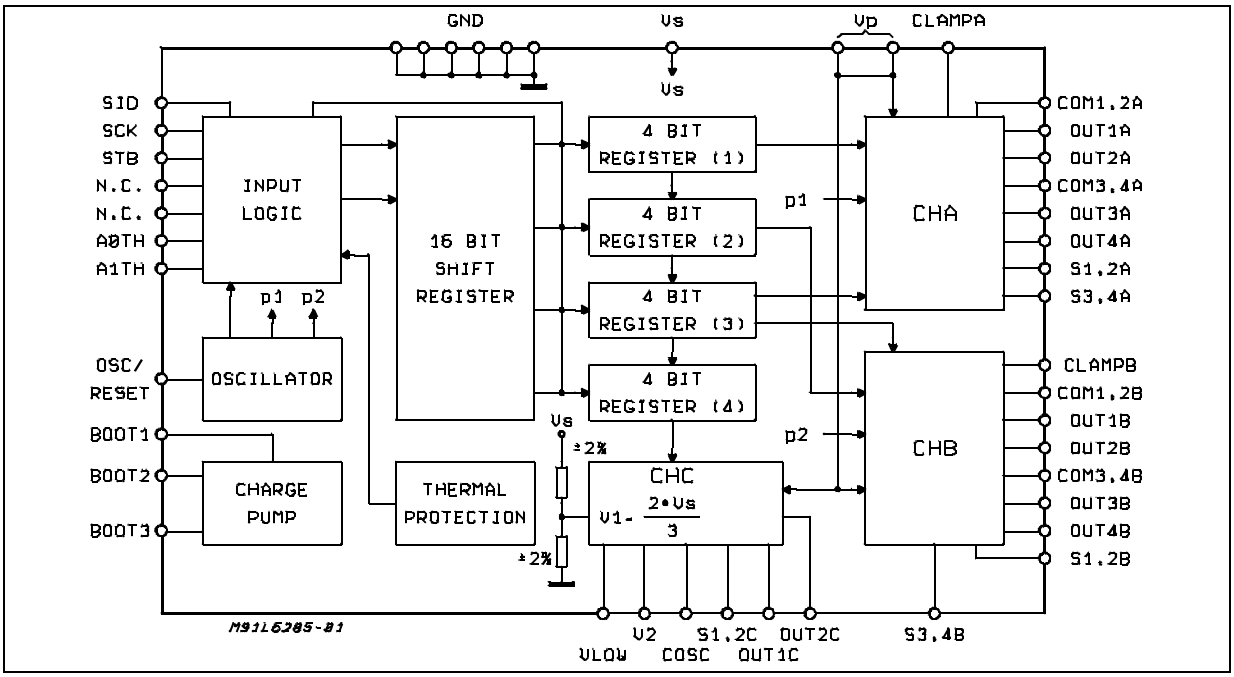
1) Two unipolar stepper motor driver
2) A full bridge DC motor driver
3) Serial microprocesor interface

The power output stages are DMOS and the input can be interfaced to a CMOS Microprocessor logic.

The phase current in the unipolar stepper motor windings is controlled by two external sensing resistors in fixed frequency chopping mode. The oscillator block provides clocks each other 180° out of phase to the two stepper motor driver in order to avoid symultaneous current peaks.

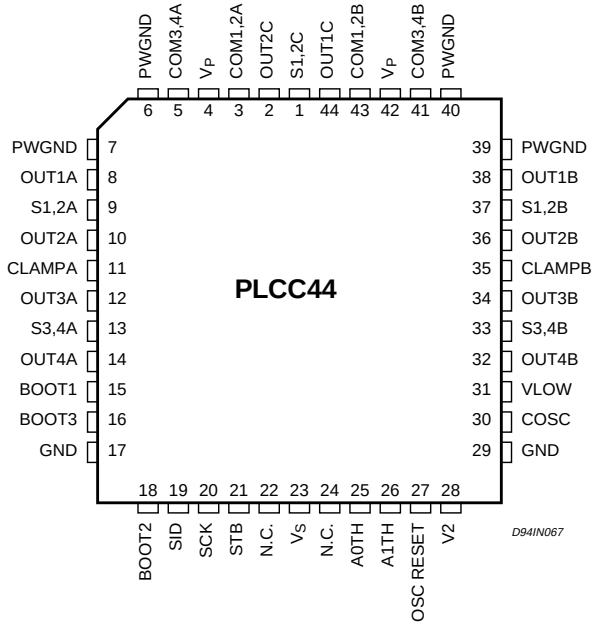
For the DC motor driver is used a bridge; the RMS voltage to supply this motor is fixed by a

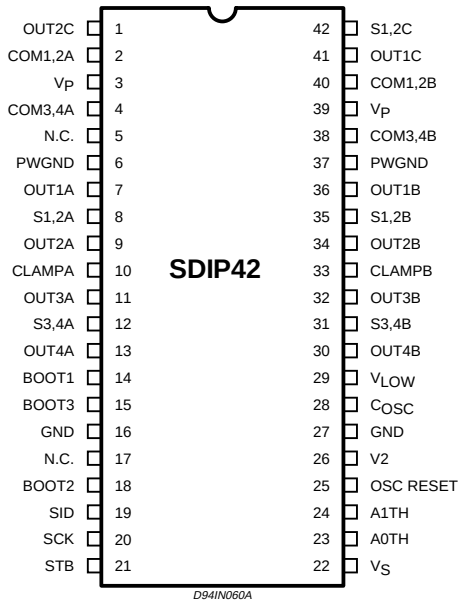
### BLOCK DIAGRAM



simple PWM open loop. The 3 motors are controlled by the micro through 4 latches of 4 bit each. The loading of these registers is in serial mode. The I.C. operates at 5V supply for the logic and at 24V supply for the power stages. The packages are SDIP42 and PLCC44 with 6 pins devoted to ground and to sink out the heat produced by power dissipation.

**PIN CONNECTION** (Top view)




## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_P$ | Power Supply Voltage | 30 | V |
| $V_S$ | Logic Supply Voltage | 7 | V |
| $V_{in}$ | Logic Input Voltage | -0.3 to $V_S$ + 0.3 | V |
| $I_{LOW}$ | Low Side DMOS max DC Current | 1 | A |
| $I_{HIGH}$ | High Side DMOS max DC Current | 1 | A |
| $I_{pLOW}$ | Low Side DMOS max Peak Current (1µs On; 50µs OFF) | 2 | A |
| $I_{pHIGH}$ | High Side DMOS max Peak Current (1µs On; 50µs OFF) | 2 | A |
| $V_{bout}$ | Max Output Voltage of Stepper Motor Driver (transient rcirculation) | 60 | V |
| $V_{sense}$ 1;2 | Max Voltage ON Vsense (CHA/CHB) | -1 to 2 | V |
| $V_{sense}$ 3 | Max Voltage ON $V_{sense}$ (CHC) | -1 to 2 | V |
| $I_{fdDC}$ | Max DC Current of Forward Diode (DMOS Source Drain Diode) | 1 | A |
| $I_{fdpk}$ | Max Peak Current of Forward Diode (DMOS Source Drain Diode) (1µs On; 50µs OFF) | 2 | A |
| $P_{tot}$ | Total Power Dissipation (Tpins = 90°C)<br>With minimized dissipating copper area ($T_{amb}$ = 70°C) | 5<br>1.6 | W<br>W |
| $T_{op}$ | Operating Temperature Range | 0 to 150 | °C |
| $T_{stg}$ | Storage Temperature Range | -40 to 150 | °C |

## THERMAL DATA (PLCC44)

| Symbol | Description | | SDIP42 | PLCC44 | Unit |
|---|---|---|---|---|---|
| $R_{th\ j\text{-}pins}$ | Thermal Resistance Junction-pins | Max. | 15 | 12 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal Resistance Junction-ambient | Max. | 48 | 50 | °C/W |

## PIN DESCRIPTION

| SDIP42 N° | PLCC44 N° | Name | Functions |
|---|---|---|---|
| 42 | 1 | S1,2C | Full bridge common source output to separate between power GND and logic GND. |
| 1,41 | 2,44 | OUT 1C, OUT 2C | Output of the channel C bridge. |
| 2 | 3 | COM 1,2A | High side DMOS channel A for current chopping in the windings connected pins to OUT 1A, OUT 2A. |
| 3,39 | 4,42 | $V_p$ | Power Supply Voltage. |
| 4 | 5 | COM 3,4A | High side DMOS channel A for current chopping in the windings connected to pins OUT 3A, OUT 4A. |
| 6,37 | 6,7,39,40 | GND | PowerGround and heatsink pins. |
| 7,9, 11,14 | 8,10 12,14 | OUT 1A, OUT 2A OUT 3A, OUT 4A | Low side DMOS outputs of channel A stepper motor driver. |
| 8 | 9 | S1,2A | Channel A sources of the DMOS OUT 1A, OUT 2A. A sensing resistor has to be connected from this pin and ground, for current control of phase 1,2 A. |
| 10,33 | 11,35 | CLAMP A, CLAMP B | These pins have to be connected to an external zener diode to clamp the output voltage spikes of channel A/B. |
| 12 | 13 | S3,4A | Channel A sources of the DMOS OUT 3A, OUT 4A. A sensing resistor has to be connected from this pin and ground, for current control of phase 3,4 A. |
| 14 | 15 | BOOT 1 | A capacitor between this pin and $V_p$ stores the overvoltage for each high side DMOS driver gate. |
| 15 | 16 | BOOT 3 | A capacitor between this pin and internal diodes allows the change pump to transfer energy to the capacitor at the pin BOOT 1. |
| 16,27 | 17,29 | GND | Logic Ground and Heatsink pins. |
| 18 | 18 | BOOT 2 | Charge pump oscillator output. |
| 19 | 19 | SID | Serial data input. |
| 20 | 20 | SCK | Serial clock for serial data input. |
| 21 | 21 | STB | Strobe to transfer the 16 bit shift register contents to the latch registers. |
| 5,17 | 22,24 | NC | Not connected. |
| 22,39 | 23 | $V_s$ | Logic Supply Voltage. |
| 23,24 | 25,26 | A0TH / A1TH | Open collector outputs for thermal informations to the µP. |
| 25 | 27 | OSC/ RESET | An RC network connected to this pin defines the oscillator frequency for stepper drivers. When OSC/RES is <1V, a reset signal is internally generated. |
| 26 | 28 | V2 | A voltage to this pin defines the output duty cycle of Channel C. |
| 28 | 30 | $C_{osc}$ | A capacitor connected to this pin defines the chopping frequency of channel C. |
| 29 | 31 | $V_{low}$ | This pin is low when the chopping low voltage (V2 low level) is selected; it is in high impedance when the chopping high voltage (V2 high level) is selected. Only for CHC operation. |
| 30,32, 34,36 | 32,34 36,38 | OUT4B, OUT3B OUT2B ,OUT1B | Low side DMOS outputs of channel B stepper motor driver. |
| 31 | 33 | S 3, 4B | Same as S 3, 4A, but for channel B. |
| 35 | 37 | S 1, 2B | Same as S 1, 2A, but for channel B. |
| 38 | 41 | COM 3, 4B | Same as COM 3, 4A, but for channel B. |
| 40 | 43 | COM 1, 2B | Same as COM 1, 2A, but for channel B. |

**ELECTRICAL CHARACTERISTICS** ($T_j$ = 25 °C, $V_S$ = 5V, $V_p$ = 24V unless othewise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_p$ | Power Supply Voltage | | 9 | | 26.5 | V |
| $I_p$ | Quiescent Power Supply Current | (note 1) | | | 7 | mA |
| $V_S$ | Logic Supply Voltage | | 4.5 | | 5.5 | V |
| $I_s$ | Quiescent Logic Supply Current | (note 1) | | | 20 | mA |

**LOGIC LEVEL**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{inL}$ | Input Low Voltage | | -0.3 | | 1.35 | V |
| $V_{inH}$ | Input High Voltage | | 3.15 | | $V_S$+0.3 | V |
| $I_{inL}$ | Input Low Current | $V_{in} = V_{inL}$ | -10 | | | µA |
| $I_{inH}$ | Input High Current | $V_{in} = V_{inH}$ | | | 10 | µA |

**CHANNEL A AND CHANNEL B (UNIPOLAR MOTORS)**

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{DSONL}$ | Low Side DMOS ON Res. | $I_{DS}$ = 0.7A | | | 1.2 | Ω |
| $R_{DSONH}$ | High Side DMOS ON Res. | $I_{DS}$ = 0.7A | | | 1.2 | Ω |
| $I_{DSSL}$ | Low Side DMOS Leakage Current | $V_{DS}$ = 60V; output OFF | | | 2 | mA |
| $I_{DSSH}$ | High Side DMOS Leakage Current | $V_P$ = 30V; $V_O$= 0V | -1.5 | | | mA |
| $V_{REF}$ | Voltage reference to the Comparator | LEVEL 1<br>LEVEL 2<br>LEVEL 3<br>LEVEL 4 | 100<br>220<br>340<br>465 | 125<br>250<br>375<br>500 | 150<br>280<br>410<br>535 | mV<br>mV<br>mV<br>mV |
| $T_d$ | Turn OFF Delay on HIGH Side DMOS after the Sensing Current Reach the Threshold Value | (note 2) | | | 1 | µs |
| $f_{max}$ | Max Chopping Frequency | | | | 40 | KHz |

**CHANNEL C (DC MOTORS)** (see Fig. 5)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{osc}$ | Oscillator Frequency | Cosc = 3.3nF; V1 = 2/3$V_S$ | 17 | 22 | 28 | KHz |
| DC | Duty Cycle | V2 = 1/2$V_S$ | 72 | 75 | 81 | % |
| $I_{b2}$ | Comparator Input Bias | V2 = 200mV | -1 | | | µA |
| $V_{low}$ | Open Drain Output | I = 5mA | | 0.2 | 0.4 | V |
| $R_{DSONH}$ | High Side DMOS ON Res. | $I_{DS}$ = 0.7A | | | 1.2 | Ω |
| $R_{DSONL}$ | Low Side DMOS ON Res. | $I_{DS}$ = 0.7A | | | 1.7 | Ω |
| $I_{LH}$ | HSD MOS Leakage Current | $V_P$ = 30V; $V_O$ = 0V | -1 | | | mA |
| $I_{LL}$ | LSD MOS Leakage Current | $V_O$ = 30V; $V_{sense}$ = 0V | -1.5 | | | mA |
| $V_{fddc}$ | Forward Diode DC Voltage (DMOS Diode) | $I_{fdcc}$ = 0.7A | | 1.4 | 2 | V |
| $f_{max}$ | Max Chopping Frequency | | | | 40 | KHz |
| $V_{boot}$ | Voltage on pin Boot1 | | $V_p$ +7 | | | V |
| $I_{L\ boot}$ | Leakage Current on pin Boot1 | $V_{bott} = V_p$ +12V; $V_p$ = 26.5V | | | 200 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

### OSCILLATOR (see Fig. 6)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{osc}$ | Oscillator Frequency Pin OSC/RESET | $C_{OSC}$ = 3.3nF; $R_{OSC}$ = 10KΩ | 27 | 41 | 46 | KHz |
| $T_{dsc}$ | Capacitor Discharge Time (protect dead time) | $C_{OSC}$ = 3.3nF; $R_{OSC}$ = 10KΩ (see Fig. 1) | 0.8 | 1.4 | 2 | µs |
| $V_{reset}$ | Reset Threshold Voltage | | 1 | | | V |

### INTERFACE TIMING

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| t1 | SCK Data Clock Cycle | (see Fig. 2) | 200 | | | ns |
| t2 | SCK Data Set-upTime | | 30 | | | ns |
| t3 | SCK Data Hold Time | | 20 | | | ns |
| t4 | SCK-STB Interval Time | | 30 | | | ns |
| t5 | STB Pulse Width | | 100 | | | ns |

**Note 1:** No output loaded; all register to low condition; no reset applied; $V_P$ = 26.5V; $V_S$ = 5.5V
**Note 2:** The effect of the internal filter (RC Network) is not considered.

**Figure 1:** Discharge time $t_{dsc}$ or Protection Time

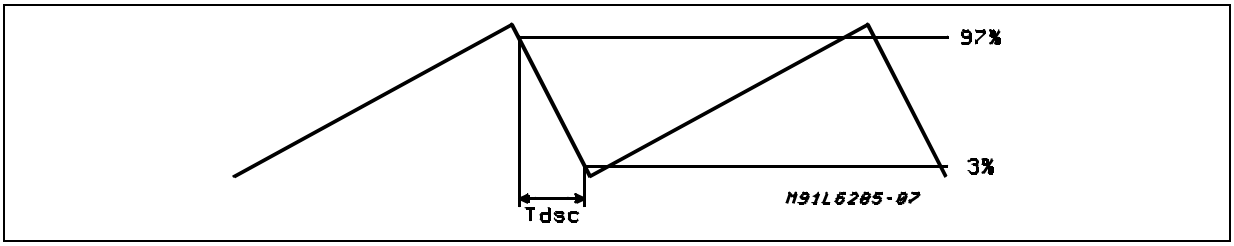
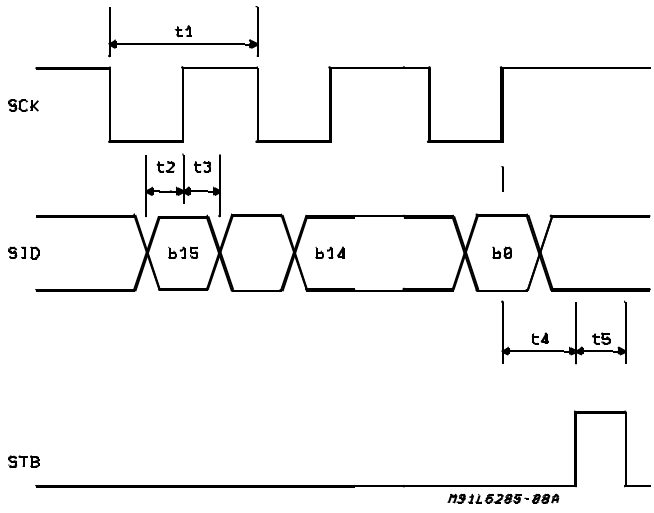



**Figure 2:** Interface Timing (Serial loading Mode)




| Serial Input Data | b15 D15 | b14 | b13 | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 | D3 | D2 | D1 | D0 |
| | Register 4 | | | | Register 3 | | | | Register 2 | | | | Register 1 | | | |

## BLOCK DIAGRAM DESCRIPTION

(see Block Diagram)

Inside the I.C. there are two unipolar stepper motor drivers, one bridge driver for DC motor, 4x4 bit latch registers, one shift register. the input logic, the charge pump, and the thermal protection.
The following conditions are valid for all the 3 driver sections:

1)When the osc/res pin is tied to GND, an internal reset signal is generated which switches off all the outputs and resets the internal registers.
2)The conditions 1 is valid also during power on and power off transitions.
3)During power on and power off, the I.C. is safe for any conditions of $V_S$ and $V_p$
3)If $V_p$ is present and $V_S$ desappears, the outputs are switched off.

### Input Logic

The input CMOS logic interfaces the microprocessor logic to the 4 registers. An integrated Schmitt-trigger circuit is used to improve noise immunity at each logic input.
The data is introduced in the 16bit shift register by the SID pin. The first bit b 15 after 16 clock applied to SCK pin will be the D15 of the shift register.

On the falling edge of STB the 16 bits of the shift register are transferred to the outputs of the 4 latch registers. Fig 2 shows the timing.

**CHA and CHB Stepper Motor Drivers**

### Registers

The Combo Motor Driver controls the 3 channels using 4 latch registers of 4 bit each:

| | | | | |
|---|---|---|---|---|
| REGISTER 1 | D0 | = | PHASE 1A | CHANNEL A |
| | D1 | = | NPHASE 2A | CHANNEL A |
| | D2 | = | PHASE 3A | CHANNEL A |
| | D3 | = | NPHASE 4A | CHANNEL A |
| REGISTER 2 | D0 | = | PHASE 1B | CHANNEL B |
| | D1 | = | NPHASE2B | CHANNEL B |
| | D2 | = | PHASE 3B | CHANNEL B |
| | D3 | = | NPHASE4B | CHANNEL B |
| REGISTER 3 | D0 | = | D/A CHANNEL A | LEAST |
| | D1 | = | D/A CHANNEL A | MOST |
| | D2 | = | D/A CHANNEL B | LEAST |
| | D3 | = | D/A CHANNEL B | MOST |
| REGISTER 4 | D0 | = | INPUT 1 | CHANNEL C |
| | D1 | = | INPUT 2 | CHANNEL C |
| | D2 | = | V2 VOLTAGE | CHANNEL C |
| | D3 | = | V2 VOLTAGE | CHANNEL C |

**Register 1/2 Output Status** (CHA and CHB) . See note 1

| D0 | D1 | D2 | D3 | OUT1 A/B | OUT2 A/B | OUT3 A/B | OUT4 A/B |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | OFF | OFF | OFF | OFF |
| 1 | 0 | 0 | 0 | ON | OFF | OFF | OFF |
| 1 | 0 | 1 | 0 | ON | OFF | ON | OFF |
| 0 | 0 | 1 | 0 | OFF | OFF | ON | OFF |
| 0 | 1 | 1 | 0 | OFF | ON | ON | OFF |
| 0 | 1 | 0 | 0 | OFF | ON | OFF | OFF |
| 0 | 1 | 0 | 1 | OFF | ON | OFF | ON |
| 0 | 0 | 0 | 1 | OFF | OFF | OFF | ON |
| 1 | 0 | 0 | 1 | ON | OFF | OFF | ON |
| ALL THE OTHERS | | | | OFF | OFF | OFF | OFF |

**Register 3 Current Reference** (D/A OUTPUT)

| DO | D1 | REFER. VOLTAGE CHANNEL A |
|---|---|---|
| 0 | 0 | 0.125 V |
| 0 | 1 | 0.250 V |
| 1 | 0 | 0.375 V |
| 1 | 1 | 0.500 V |

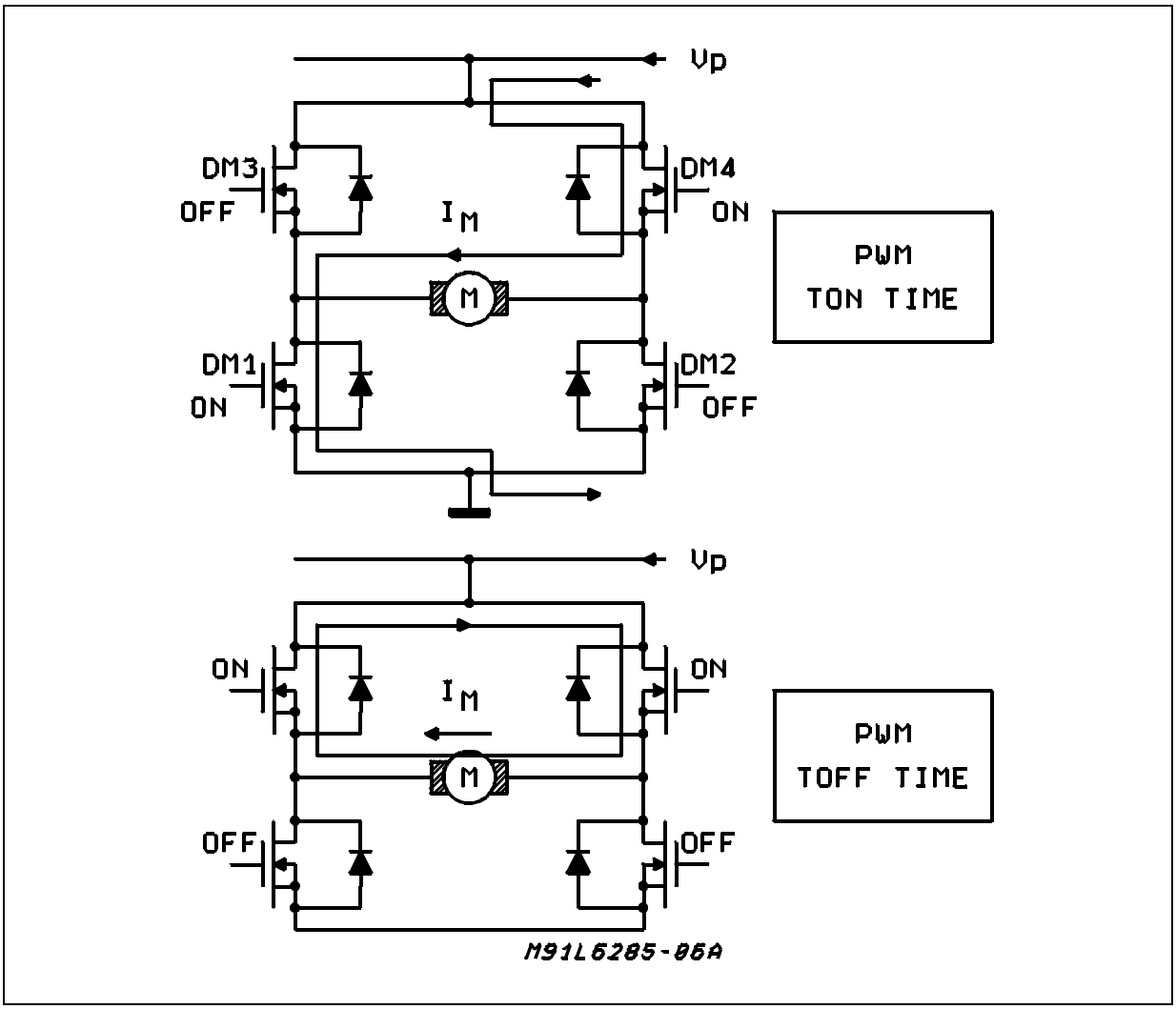
| D2 | D3 | REFER. VOLTAGE CHANNEL B |
|---|---|---|
| 0 | 0 | 0.125 V |
| 0 | 1 | 0.250 V |
| 1 | 0 | 0.375 V |
| 1 | 1 | 0.500 V |

**REGISTER 4** (CHC). See note 2

| D0 | D1 | D2 | D3 | OUT1 C | OUT2 C |
|---|---|---|---|---|---|
| X | X | 0 | 0 | OFF | OFF |
| 0 | 0 | 1 | 1 | OFF | OFF |
| 1 | 0 | 1 | 1 | $V_P$ | GND |
| 0 | 1 | 1 | 1 | GND | $V_P$ |
| 1 | 1 | 1 | 1 | GND | GND |
| 1 | 0 | 1 | 0 | $V_P$ | CHOPPING; V2 LOW LEVEL |
| 0 | 1 | 1 | 0 | CHOPPING; V2 LOW LEVEL | $V_P$ |
| 1 | 0 | 0 | 1 | $V_P$ | CHOPPING; V2 HIGH LEVEL |
| 0 | 1 | 0 | 1 | CHOPPING; V2 HIGH LEVEL | $V_P$ |
| 0 | 0 | 1 | 0 | OFF | OFF |
| 1 | 1 | 1 | 0 | $V_P$ | $V_P$ |
| 0 | 0 | 0 | 1 | OFF | OFF |
| 1 | 1 | 0 | 1 | $V_P$ | $V_P$ |

**Note 1:** Low side DMOS status (DM1/2 in Fig. 4)
**Note 2:** Bridge status (see Fig. 3): OFF = tristate; $V_P$ =, DM3/4ON; GND = DM1/2 ON

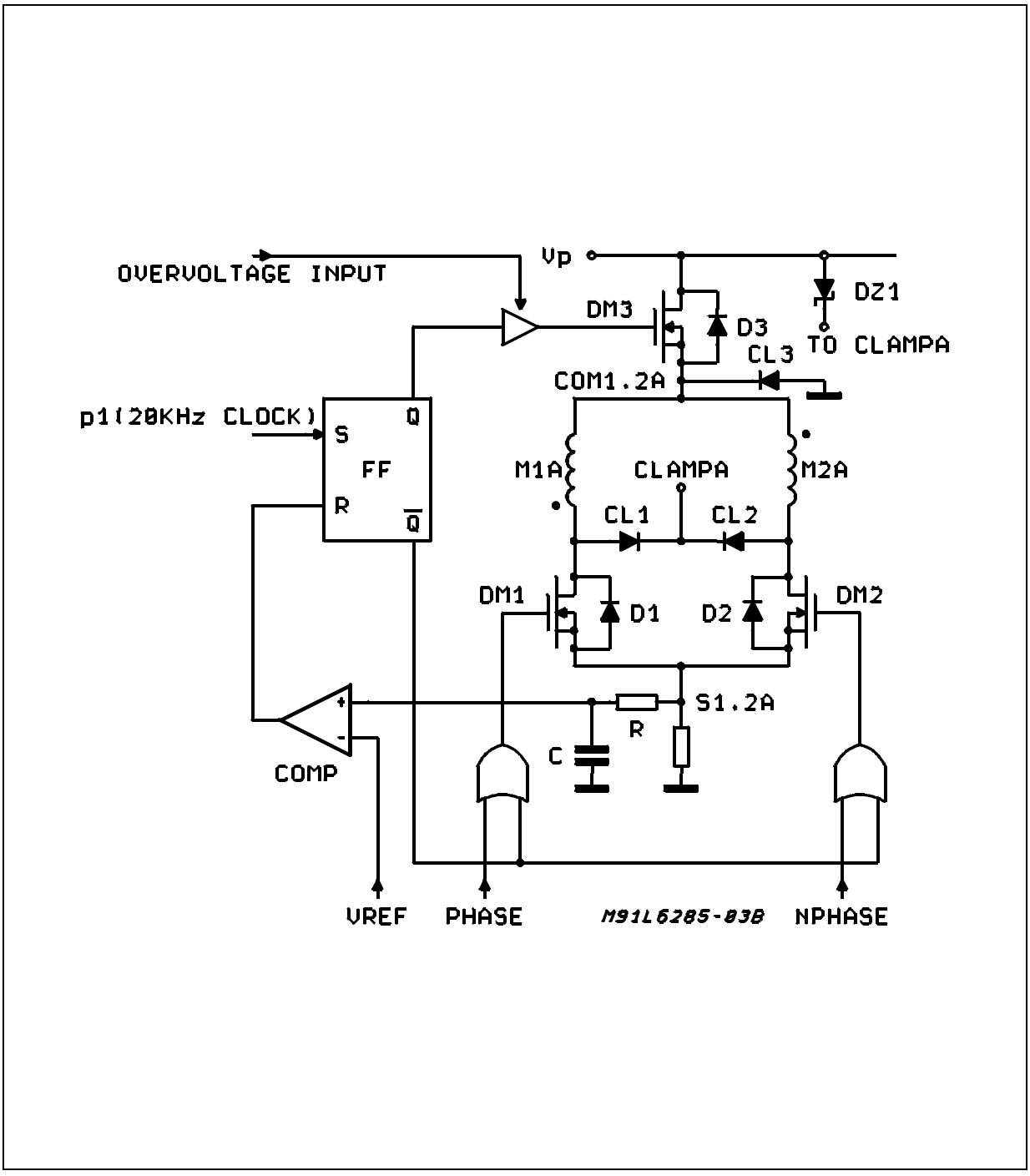
**Figure 3:** CHC Chopping Characteristics



These two channels drive two unipolar stepper motors in chopping mode. The basic channel configuration is shown in Fig 4. by considering well known the PWM Current Control Loop behaviour here below only particular trick are underlined. During DM3 off period the low side DMOS DM1 and DM2 are switched on to reduce the power dissipation.

The drain overvoltages generated because of the stray inductance of the motor windings are limited by connecting the DZ1 external zener diode to the clamp pin.. The diodes CL1 and CL2 are integrated as far as the CL3 diode which limits the negative voltage at pin COM1.2. An internal RC network (1µs) is realized to filter the sensing resistor signal.

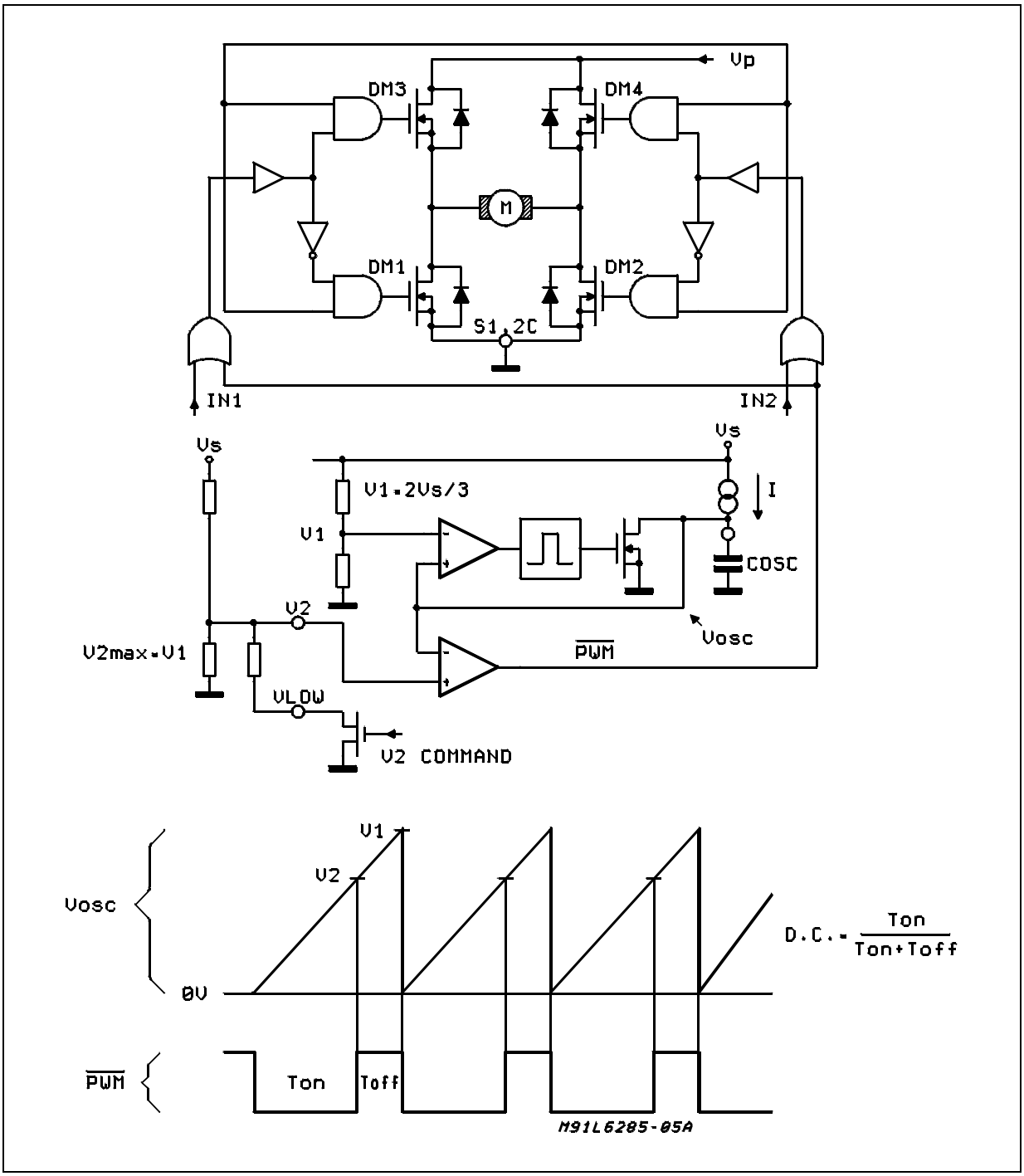
**Figure.4**: Unipolar motor driver CHA (or CHB)



**CHC DC Motor Driver**

The DC motor driver is a DMOS full bridge with a PWM Open Loop Voltage Control. Fig.5 shows the theory of operation. The $C_{osc}$ Capacitor is charged by a constant current source. The oscillating voltage value is from 0V to the V1 level internally fixed at V1 = 2/3 $V_S$. The output duty cycle is controlled by the V2 voltage. The operational range of V2 is from 200mV to V1. Fig.3 shows the DMOS status during PWM: $t_{ON}$ and $t_{OFF}$ bridge configurations. While the PWM Duty Cycle defines the motor speed (not controlled since the loop is open),the logic level of IN1 and IN2 can choose the direction of the motor.

**Figure.5:** DC Motor Driver CHC



**Oscillator For Clock and Reset Generation**

The oscillator block provides for two functions:

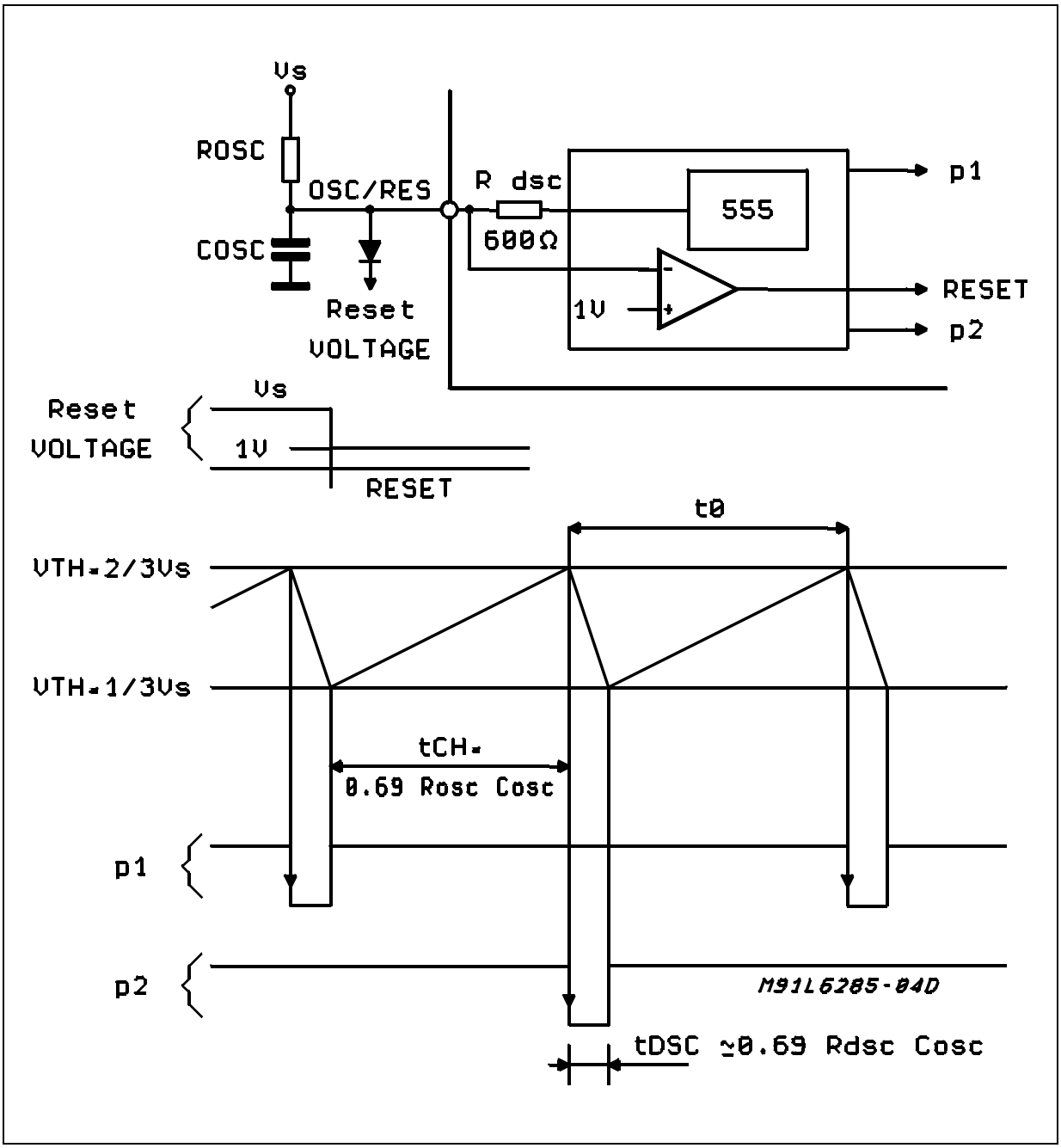
1)Generate an internal reset signal when the voltage at pin osc/res is below 1V. The reset signal switches off all the outputs and resets the logic registers.

2)Generate, when the pin osc/res is left free two syncro signals p1 and p2 for the clock of the PWM Current Control of the two stepper driver blocks

The oscillator operates like the 555 concept in which the capacitor voltage oscillates between $1/3V_S$ $2/3V_S$ (Fig. 6). The oscillator frequency is 2 times the chopping frequency in order to generate the two syncro signals at operative 20KHz PWM. The $t_{CH}$ = charge time of Cosc is defined by $R_{osc}$, $V_{TH1}$ and $V_{TH2}$ ( threshold voltages)and $C_{osc}$.

The discharge time $T_{dsc}$ is practically only defined by Cosc and the internal discarge resistor Rdsc. The $t_{dsc}$ is also the time lockout during which the RS FF cannot read the Comparator output (see Fig. 4)

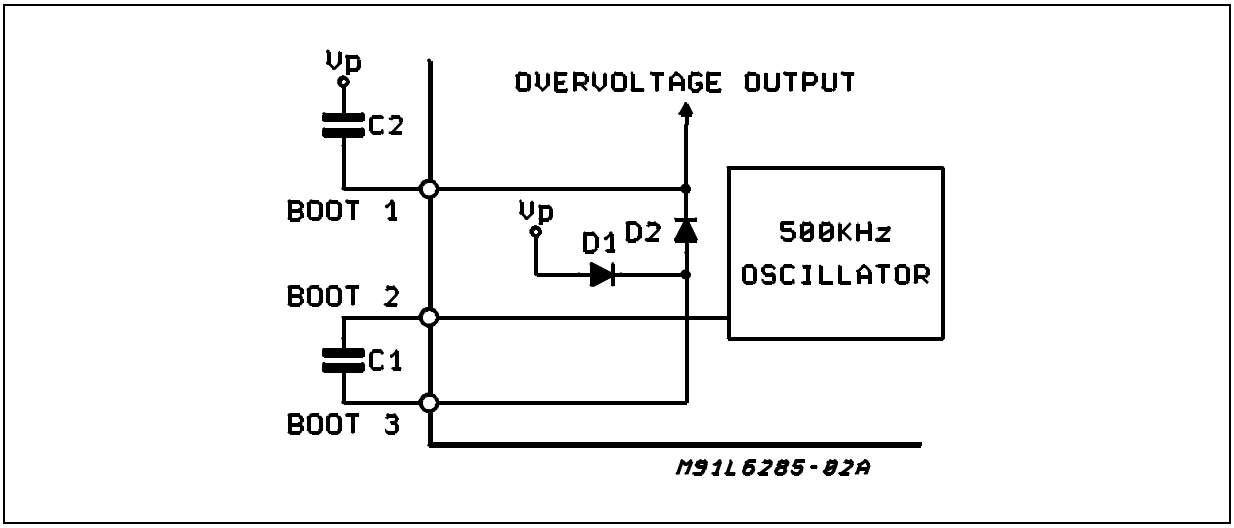
**Figure 6**: Oscillator Concept



### Charge Pump

The charge pump circuitry generates the overvoltage needed to drive the gate of the high side output DMOS power transistors.It is realized by using two external capacitors (C1 and C2) and two integrated diodes that operate as a full wave rectifier (see Fig. 7). The oscillator peak to peak output voltage is stored by C2 and summed to the Power Supply Voltage $V_p$..
The voltage present at the pin BOOT1, is then the overvoltage needed to supply the gate of the high side DMOS drivers.

**Figure 7:** Charge Pump Circuit




### THERMAL PROTECTION

The thermal protection shuts down the chip before it can reach a dangerous temperature.
Additional informations to the microprocessor are available at the A0TH, A1TH pins.

| A0TH | A1TH | THERMAL PROTECTION | CIRCUIT STATUS |
|---|---|---|---|
| 0 | 0 | OK | OPERATING |
| 1 | 0 | PREALARM | OPERATING |
| 1 | 1 | ALARM | THERMAL SHUTDOWN |
| 0 | 1 | NOT POSSIBLE | |

### APPLICATION INFORMATION

A typical application circuit is shown in Fig.8. By this application it is possible to drive two unipolar stepper motors (M1,M2) and one DC motor (M3). As it can be seen, only two external Zener diodes (D1,D2) are needed to clamp the voltage transients generated by the stray inductance of the motor windings. This is recommended when the peak current is not more than three to four hundred mAmps. For a power supply voltage of $V_P$=24V ±10%, D1=D2 must be 30V ±5%-1W (1N4751A or equivalent). Both the $V_P$ and the $V_S$ pins need bypass capacitors (C1,C2,C3); to supply the high-side DMOS (Source Transistors) at pin.15 ,only two external capacitors (C4,C5) complete the charge pump circuitry. The oscillator frequency, that is twice the chopping frequency for M1 and M2, is mainly defined by the network R6C6:

$f_{osc} = [0.69 (R_{ch} + Rd_{sc}) C_{osc}]^{-1}$ , where

$R_{ch}$ = R6 ; $R_{dsc}$ = 600 ohm typ.

At the same time, the lockout duration (or protection window) needed for a correct chopping behavior, is given by :

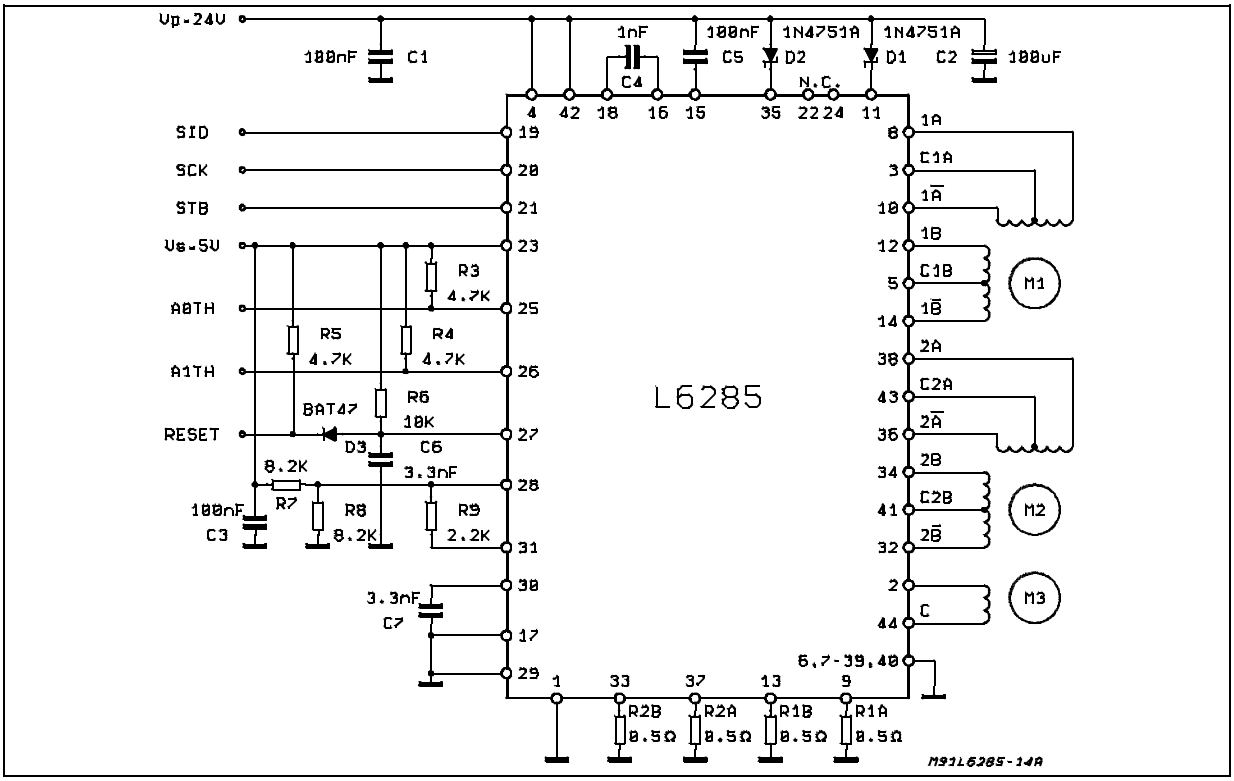
$T_{lockout} = 0.69 R_{dsc} C_{osc}$

The shown values (fig.8) give a nominal frequency a little bit more than 41KHz and a protection window of 1.4 µs roughly. The Schottky diode D3 and the pull-up resistor R5 driven via an open-collector transistor can generate the Reset function. The chopping current is sensed across R1 A/B; R2 A/B that must be of a not inductive type. The DC motor PWM Open Loop Voltage Control operates at a frequency defined by C7, charged with a typical constant current source (I = 240 µA), up to V1 = 0.67 $V_S$. Since the discharge time is very short, it can be written :

$f_{osc} = I / C_{osc} V1$, where $C_{osc}$ = C7.

Tha values indicated in figure give a typical frequency of about 22 KHz.

**Figure 8:** Typical Application Circuit




The duty cycle DC can be chosen between two possibilities (High and Low ) than can be defined externally by the resistors R7, R8 and R9: Fig.5 let well understand how to calculate the dividers that fix V2 H (wider $t_{on}$ ) and V2 L (wider $t_{off}$ ). It may be needed to drive stepper motors that require a higher peak current than told above. In this case each motor phase requires a particular application arrangement (see Fig.9b). In Fig.9a all the protection components are integrated with the exception of Z1. In Fig.9b the clamp of the voltage spikes generated by the stray inductance Ls is achieved using Transil protection T1 and T2 that works also as additional diodes during current recirculation at the phase change. The diode D1, externally connected, is recommended at the highest working current levels and/or when the supplied voltage (plus Back EMF) at the end of the motor winding is too much unbalanced.

**Figure 9a:** Output Configuration as it is obtained by the Application Circuit

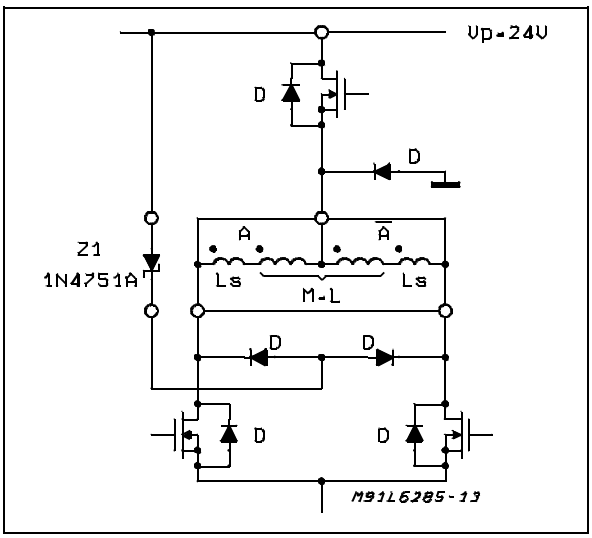
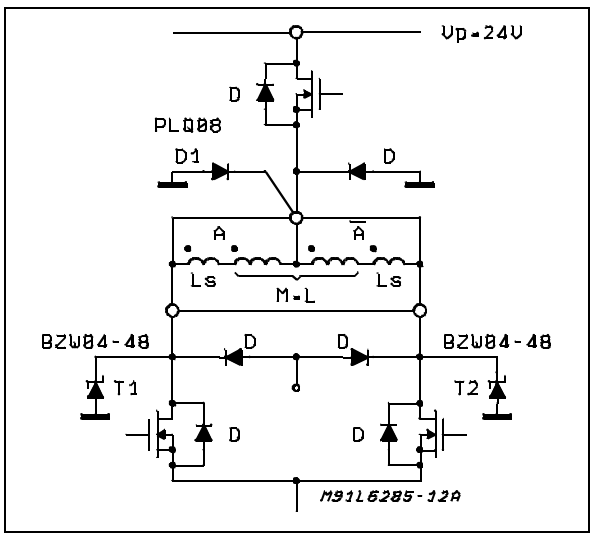



**Figure 9b:** Output Configuration at Higher Operating Currents



## THERMAL CHARACTERISTICS

The cooling of the device is obtained by soldering its ground pins on a proper p.c.b copper side , acting as a true heatsink. By considering four squared side as in Fig.10, the junction to ambient thermal resistance has been measured (see Fig.11). The typical transient thermal resistance versus values of single pulse width of power is shown in Fig.12. In general these thermal characteristics are very important to the designer to optimize the L6285 applications.

**Figure 10:** Four "on board" Square Heatsink

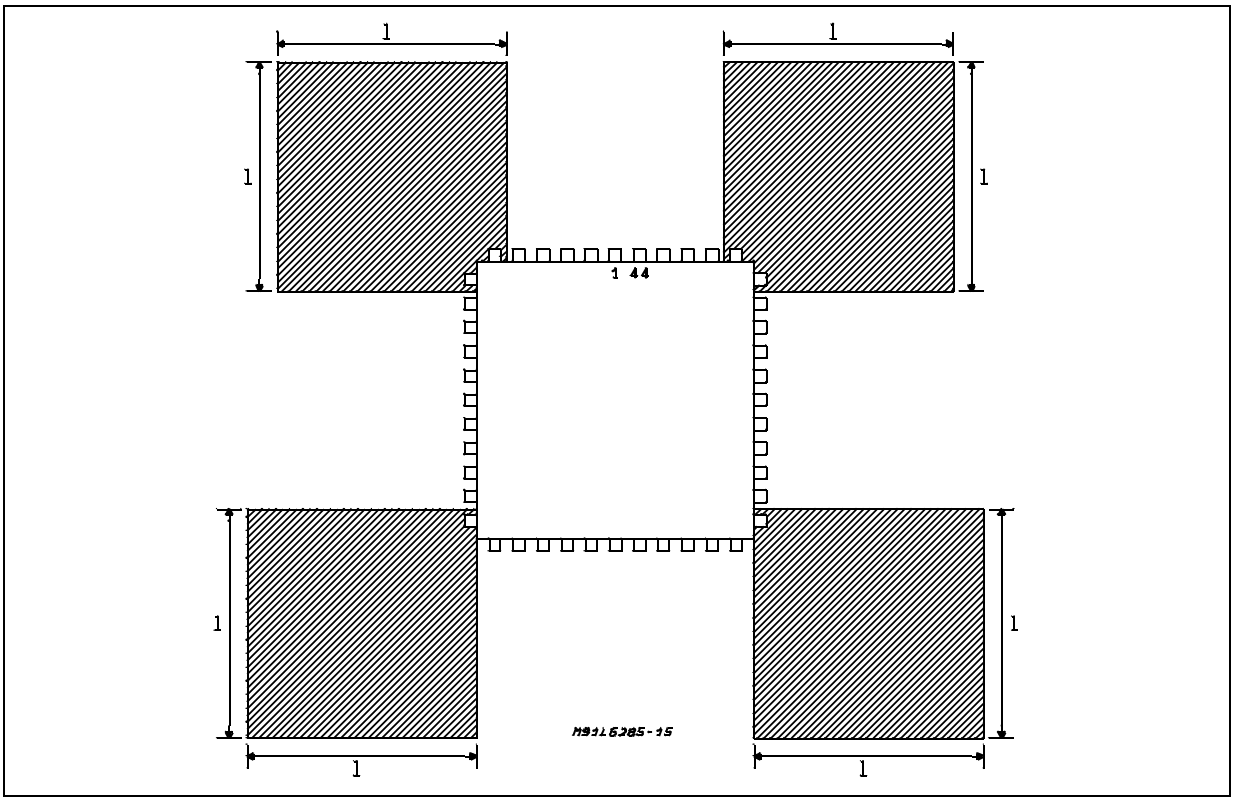



**Figure 11:** Typical $R_{th\ j\text{-}amb}$ vs. lenght "l" (Fig. 10)

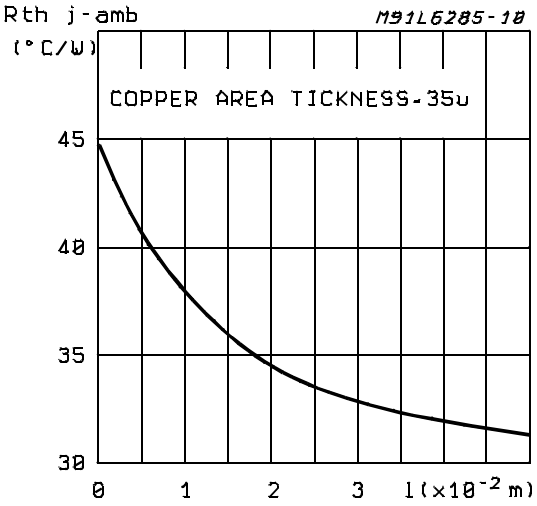
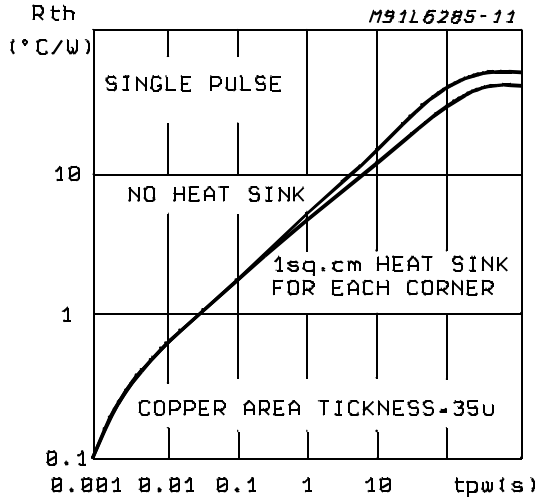
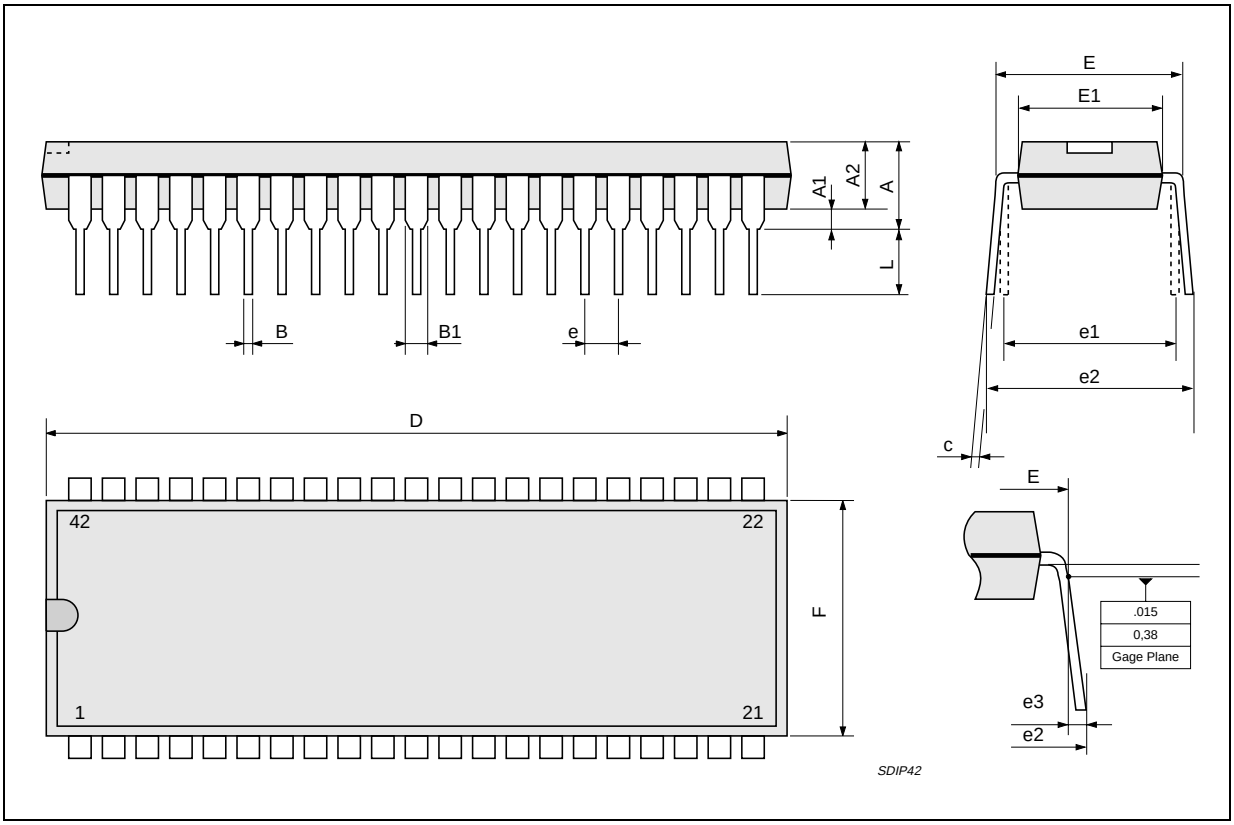



**Figure 12:** Typical Transient Thermal Resistance vs. Time or Pulse Width



## SDIP42 PACKAGE MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 5.08 | | | 0.20 |
| A1 | 0.51 | | | 0.020 | | |
| A2 | 3.05 | 3.81 | 4.57 | 0.120 | 0.150 | 0.180 |
| B | 0.36 | 0.46 | 0.56 | 0.0142 | 0.0181 | 0.0220 |
| B1 | 0.76 | 1.02 | 1.14 | 0.030 | 0.040 | 0.045 |
| c | 0.23 | 0.25 | 0.38 | 0.0090 | 0.0098 | 0.0150 |
| D | 37.85 | 38.10 | 38.35 | 1.490 | 1.50 | 1.510 |
| E | 15.24 | | 16.00 | 0.60 | | 0.629 |
| E1 | 12.70 | 13.72 | 14.48 | 0.50 | 0.540 | 0.570 |
| e | | 1.778 | | | 0.070 | |
| e1 | | 15.24 | | | ‘0.60 | |
| e2 | | | 18.54 | | | 0.730 |
| e3 | | | 1.52 | | | 0.060 |
| L | 2.54 | 3.30 | 3.56 | 0.10 | 0.130 | 0.140 |



## PLCC44 PACKAGE MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 17.4 | | 17.65 | 0.685 | | 0.695 |
| B | 16.51 | | 16.65 | 0.650 | | 0.656 |
| C | 3.65 | | 3.7 | 0.144 | | 0.146 |
| D | 4.2 | | 4.57 | 0.165 | | 0.180 |
| d1 | 2.59 | | 2.74 | 0.102 | | 0.108 |
| d2 | | 0.68 | | | 0.027 | |
| E | 14.99 | | 16 | 0.590 | | 0.630 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 12.7 | | | 0.500 | |
| F | | 0.46 | | | 0.018 | |
| F1 | | 0.71 | | | 0.028 | |
| G | | | 0.101 | | | 0.004 |
| M | | 1.16 | | | 0.046 | |
| M1 | | 1.14 | | | 0.045 | |