

54F/74F534 Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'F534 is a high speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

Features

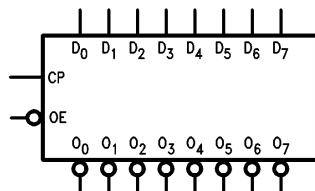
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F534PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F534DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F534SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F534SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F534FM (Note 2)	W20A	20-Lead Cerpack
	54F534LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

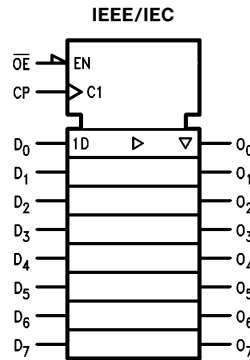
Note 1: Devices also available in 13" reel. Use suffix = SCX, and SJX

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB

Logic Symbols



TL/F/9549-1



TL/F/9549-5

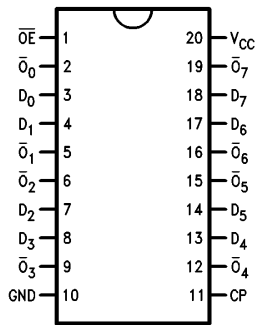
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 - D_7	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ -0.6 mA
\overline{OE}	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ -0.6 mA
\overline{O}_0 - \overline{O}_7	Complementary TRI-STATE Outputs	150/40(33.3)	-3 mA/24 mA (20 mA)

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

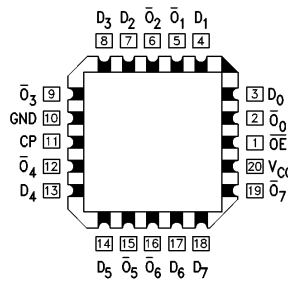
Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



TL/F/9549-2

Pin Assignment
for LCC



TL/F/9549-3

Functional Description

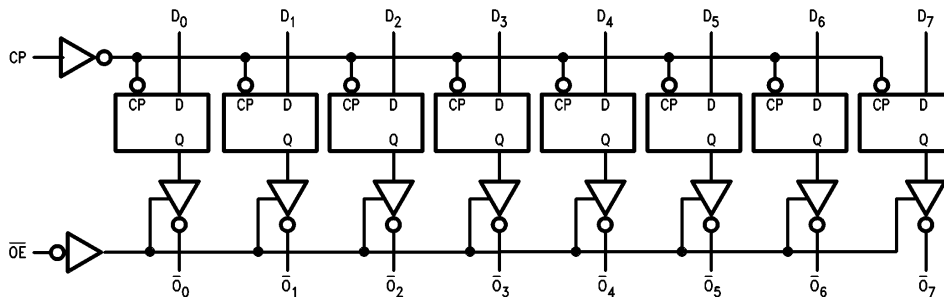
The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

Inputs			Output
CP	OE	D	\overline{O}
—	L	H	L
—	L	L	H
L	L	X	\overline{O}_0
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
— = LOW-to-HIGH Clock Transition
Z = High Impedance
 \overline{O}_0 = Value stored from previous clock cycle

Logic Diagram



TL/F/9549-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Military	-55°C to +125°C
Commercial	0°C to +70°C

Supply Voltage

Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage					V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage					V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min		I _{OH} = -1 mA
		54F 10% V _{CC}	2.4					I _{OH} = -3 mA
		74F 10% V _{CC}	2.5					I _{OH} = -1 mA
		74F 10% V _{CC}	2.4					I _{OH} = -3 mA
		74F 5% V _{CC}	2.7					I _{OH} = -1 mA
		74F 5% V _{CC}	2.7					I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC}			V	Min		I _{OL} = 20 mA
		74F 10% V _{CC}						I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F	20.0		μA	Max		V _{IN} = 2.7V
		74F	5.0					
I _{BVI}	Input HIGH Current Breakdown Test	54F	100		μA	Max		V _{IN} = 7.0V
		74F	7.0					
I _{CEX}	Output HIGH Leakage Current	54F	250		μA	Max		V _{OUT} = V _{CC}
		74F	50					
V _{ID}	Input Leakage Test	74F	4.75		V	0.0		I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F	3.75		μA	0.0		V _{IOD} = 1.50 μA All Other Pins Grounded
I _{IL}	Input LOW Current		-0.6		mA	Max		V _{IN} = 0.5V
I _{OZH}	Output Leakage Current		50		μA	Max		V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current		-50		μA	Max		V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		-60		mA	Max		V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test		500		μA	0.0V		V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current		55	86	mA	Max		V _O = HIGH Z

AC Electrical Characteristics

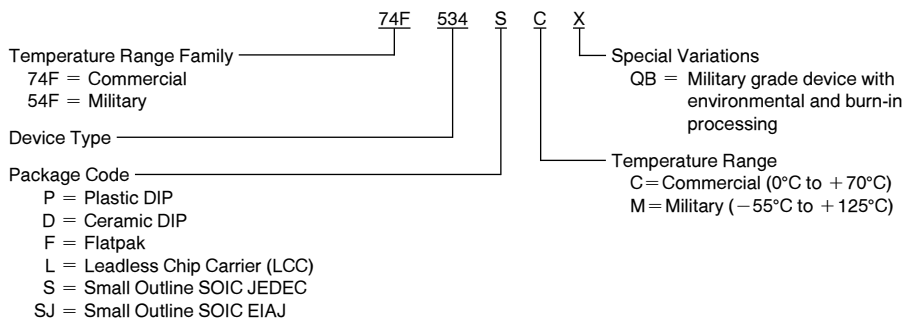
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100			60		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to \bar{O}_n	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns
t_{PZH} t_{PZL}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	5.3	7.0	1.5	8.0	1.5	8.0	ns
		1.5	4.3	5.5	1.5	7.5	1.5	6.5	

AC Operating Requirements

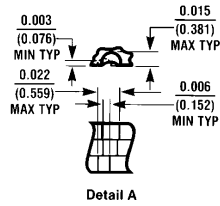
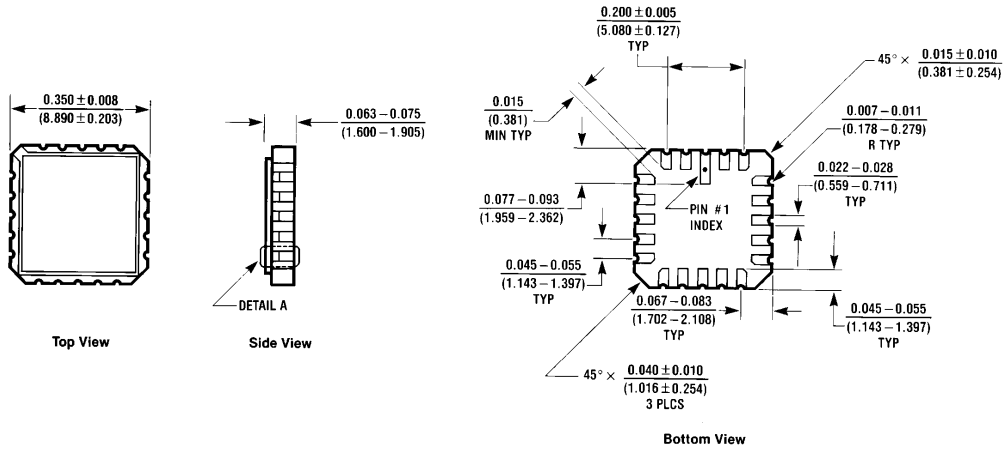
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW D_n to CP	2.0		2.0		2.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW D_n to CP	2.0		2.0		2.0		
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	7.0		7.0		7.0		ns
		6.0		6.0		6.0		

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

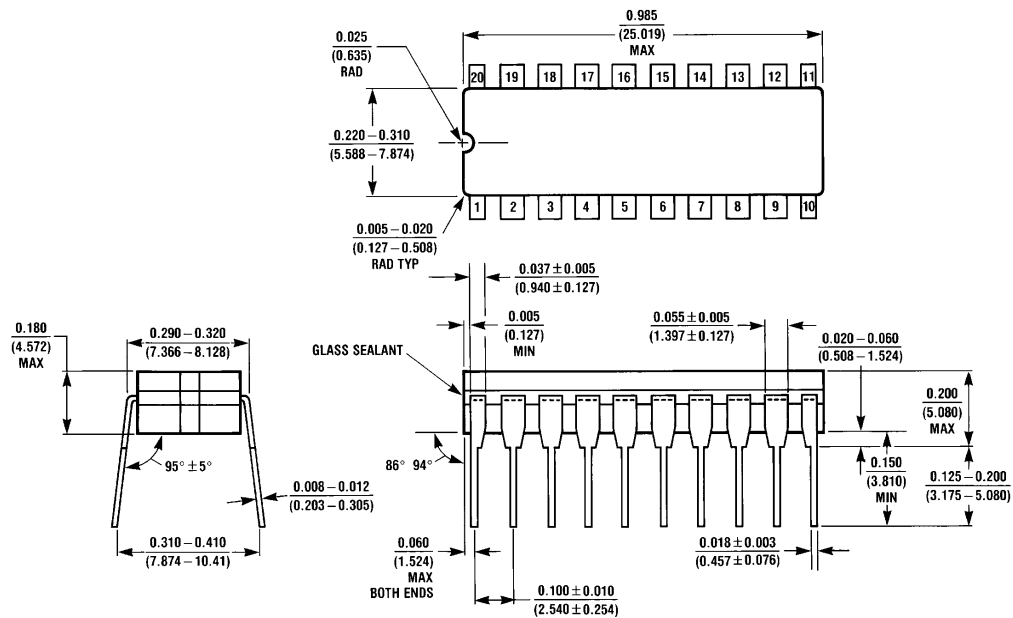


Physical Dimensions inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)
 NS Package Number E20A**

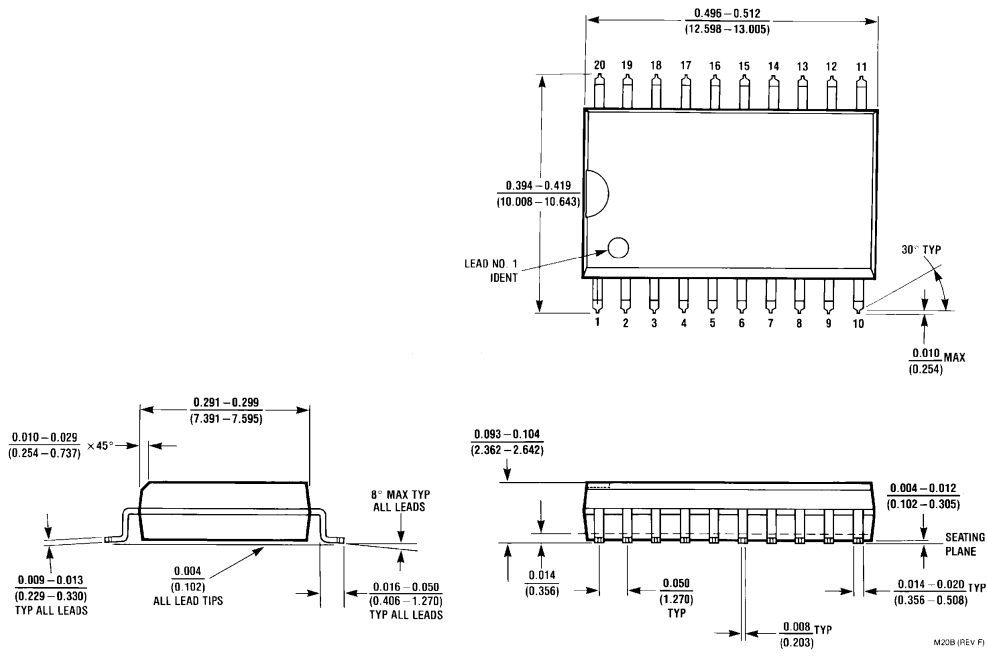
E20A (REV D)



**20-Lead Ceramic Dual-In-Line Package (D)
 NS Package Number J20A**

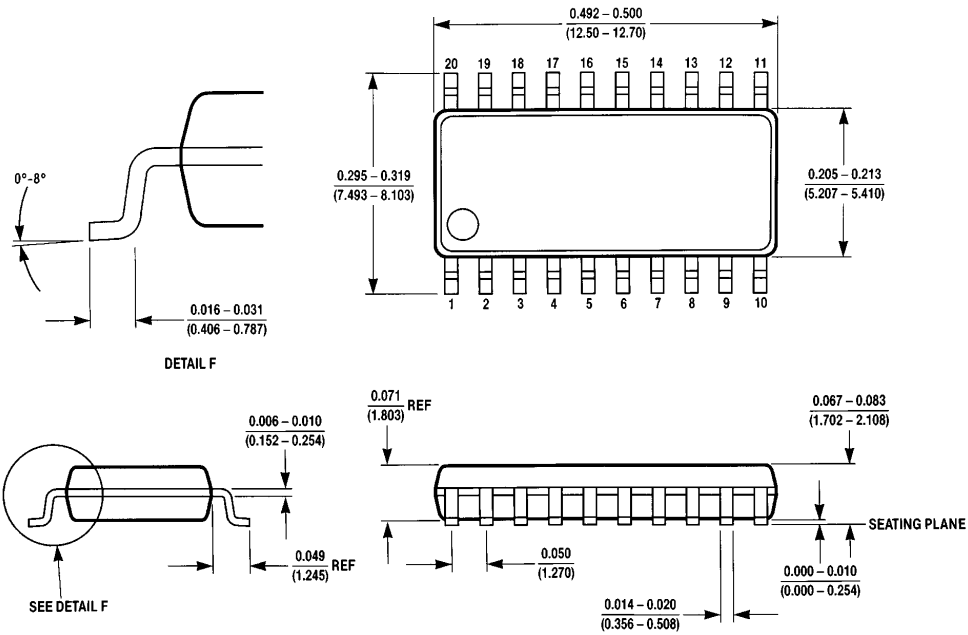
J20A (REV M)

Physical Dimensions inches (millimeters) (Continued)



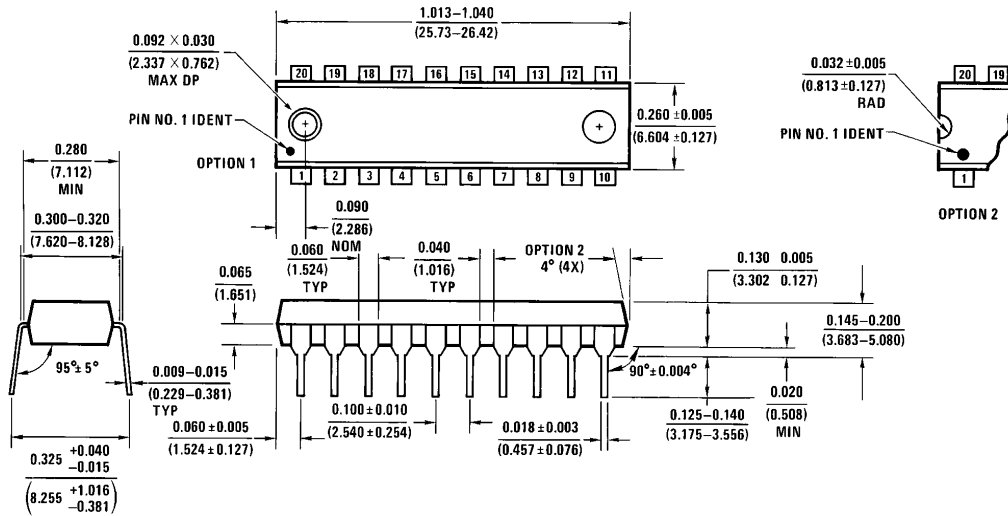
**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B**

Physical Dimensions inches (millimeters) (Continued)



M20D (REV A)

**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D**



N20A (REV G)

**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A**

Physical Dimensions inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)
NS Package Number W20A**

W20A (REV E)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.