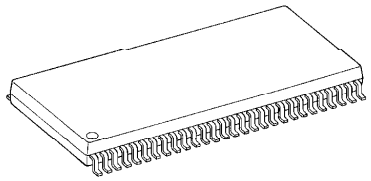
ADVANCE INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16827FT

LOW-VOLTAGE 20-BIT BUS BUFFER
WITH 3.6V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16827FT is a high performance CMOS 20-bit BUS BUFFER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.
It is also designed with over voltage tolerant inputs and outputs up to 3.6V.
The TC74VCX16827FT is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($1\overline{OE1}$ and $1\overline{OE2}$ or $2\overline{OE1}$ and $2\overline{OE2}$) inputs must both be low for the corresponding Y outputs to be active.
When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3 – state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge.



TSSOP56-P-0061-0.50

Weight : 0.25g (Typ.)

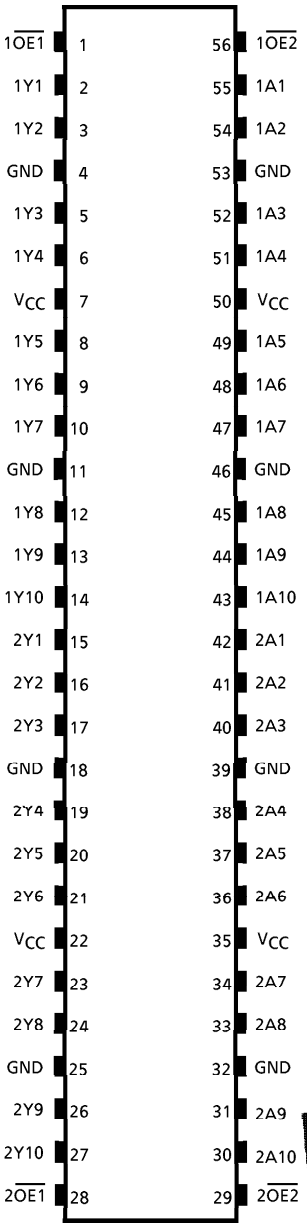
PRELIMINARY

FEATURES

- Low Voltage Operation : V_{CC} = 1.8~3.6V
- High Speed Operation : t_{pd} = TBD (max.) at V_{CC} = 3.0~3.6V
  : t_{pd} = TBD (max.) at V_{CC} = 2.3~2.7V
  : tpd = TBD (max.) at V_{CC} = 1.8V
- 3.6V Tolerant inputs and outputs.
- Output Current : I_{OH} / I_{OL} = ±24mA (min.) at V_{CC} = 3.0V
  : I_{OH} / I_{OL} = ±18mA (min.) at V_{CC} = 2.3V
  : I_{OH} / I_{OL} = ±6mA (min.) at V_{CC} = 1.8V
- Latch-up Performance : ±300mA
- ESD Performance : Human Body Model > ±2000V
  : Machine Model > ±200V
- Package : TSSOP
  (Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.

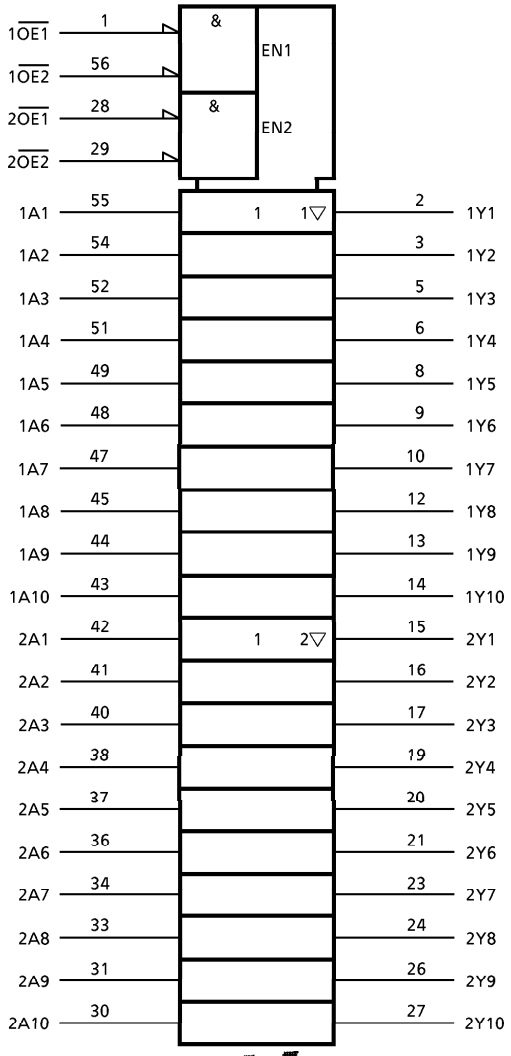
961001EBA2

PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



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FUNCTION TABLE (each 10-bit latch)

INPUT			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

SYSTEM DIAGRAM