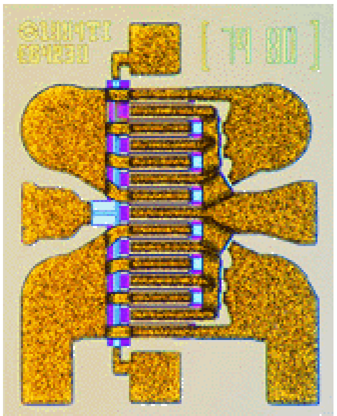
TriQuint SEMICONDUCTOR®

Product Data Sheet

March 20, 2001

Discrete HFET

TGF4230-EEU



Key Features and Performance

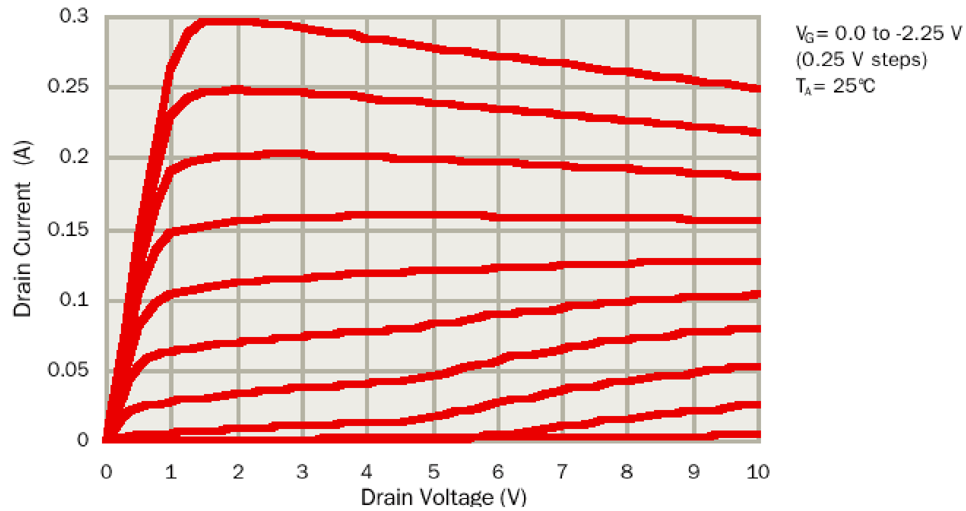
- 1200 µm x 0.5 µm HFET
- Nominal Pout of 28.5 dBm at 8.5 GHz
- Nominal Gain of 10.0 dB at 8.5 GHz
- Nominal PAE of 55 % at 8.5 GHz
- Suitable for high reliability applications
- 0.609 x 0.736 x 0.102 mm
  (0.024 x 0.029 x 0.004 in)

DESCRIPTION

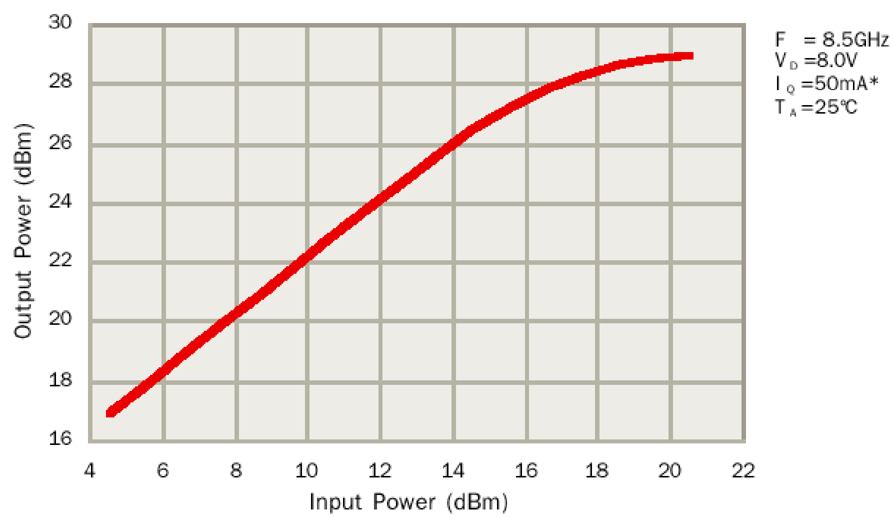
The TriQuint TGF4230-EEU is a single gate 1.2 mm Discrete GaAs Heterostructure Field Effect Transistor (HFET) designed for high-efficiency power applications up to 12 GHz in Class A and Class AB operation.

Bond-pad and backside metalization is gold plated for compatibility with eutectic alloy attach methods as well as thermocompression and thermosonic wire-bonding processes. The TGF4230-EEU is readily assembled using automatic equipment.

EXAMPLE OF DC I-V CURVES

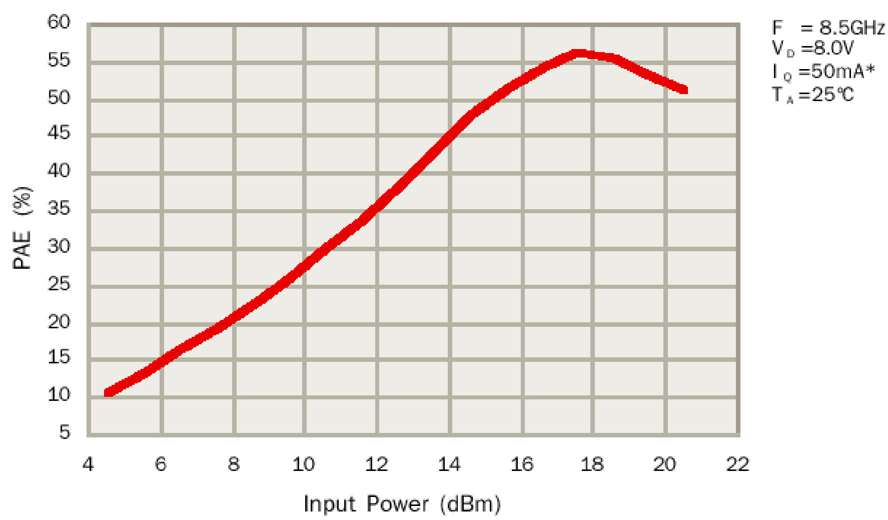


OUTPUT POWER VS. INPUT POWER

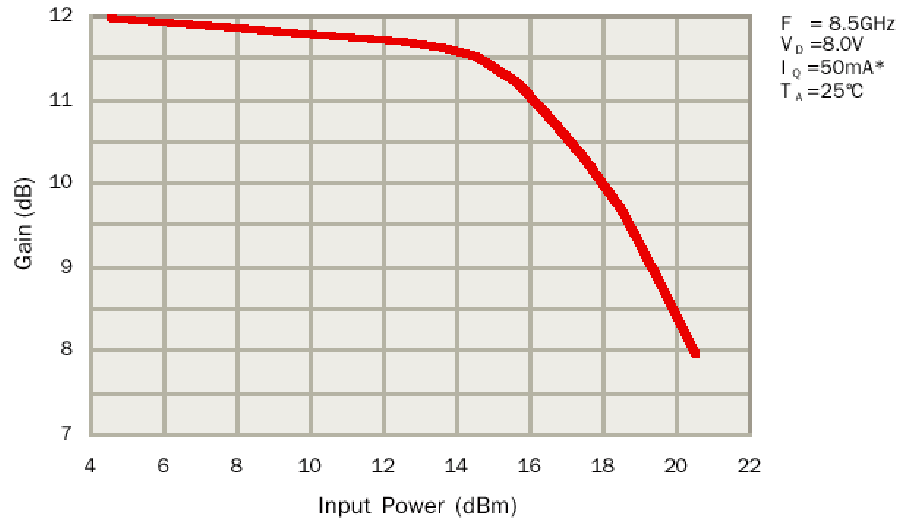


Note: I_Q is defined as the drain current before application of RF signal at the input.

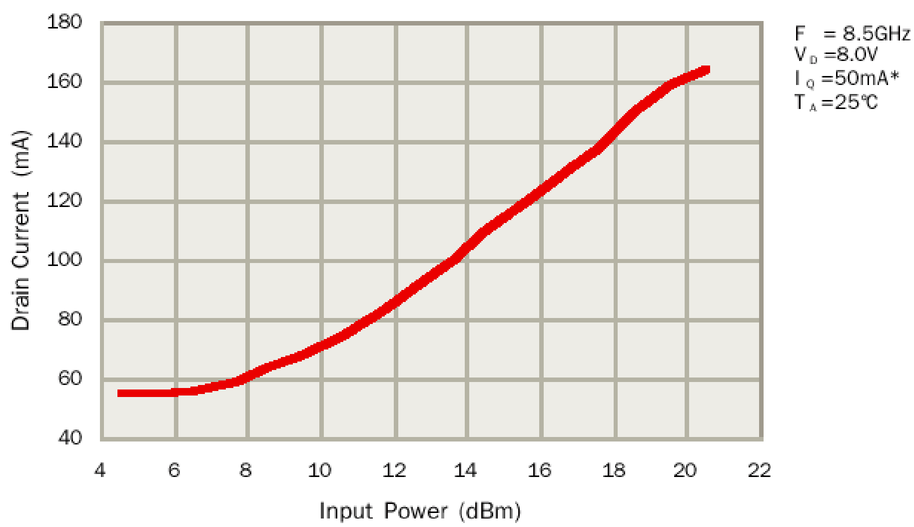
POWER ADDED EFFICIENCY VS. INPUT POWER



GAIN VS. INPUT POWER



DRAIN CURRENT VS. INPUT POWER



ABSOLUTE MAXIMUM RATINGS

Drain-to-source voltage, V_{DS} .... 12 V

Gate-to-source voltage, V_{GS} .... -5 V to 0 V

Mounting temperature (30 sec), T_M .... 320 C

Storage temperature range, T_{STG} .... -65 to 200 C

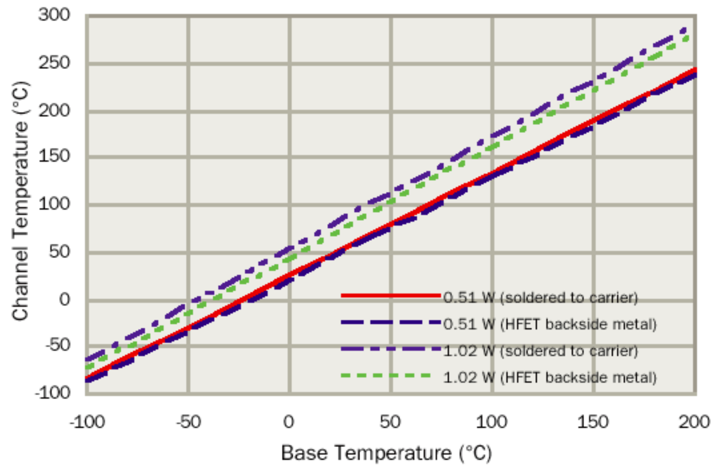
Power dissipation, P_D .... (see thermal data on next page)

Operating channel temperature, T_{CH} .... (see thermal data on next page)

Ratings over operating channel temperature (unless otherwise noted)

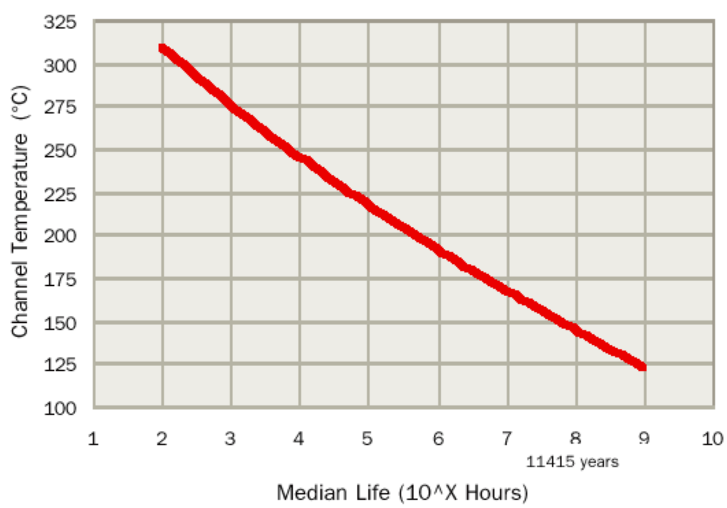
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “RF and DC Characteristics” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PREDICTED CHANNEL TEMPERATURE VS. BASE TEMPERATURE
at 0.51 W and 1.02 W dissipated power



Case 1: Base temperature at backside of carrier (with 38 µm AuSn solder attach to 0.5 mm CuMo Carrier)
Case 2: Base temperature at backside of 1.2 mm HFET.

HFET CHANNEL TEMPERATURE VS. MEDIAN LIFE



RF AND DC CHARACTERISTICS

PARAMETER		MIN	NOMINAL	MAX	UNIT
Pout	Output Power	-	28.5	-	dBm
G_P	Power Gain	-	10	-	db
PAE	Power Added Efficiency	-	55	-	%
I_{DSS}	Drain Saturation Current	204	294	384	mA
G_M	Transconductance	144	198	252	mS
V_P	Pinch-Off Voltage	-3	-1.85	-1	V
BV_{GS}	Breakdown Voltage Gate-Source	-30	-22	-19	V
BV_{GD}	Breakdown Voltage Gate-Drain	-30	-22	-19	V

Pout, Gain and PAE: These RF parameters are not measured by TriQuint. These measurements can be performed in the proposed application. Nominal values listed are at 8.5 GHz, drain voltage of 8.0 V. Gate voltage is adjusted to achieve quiescent current of approximately 20 % I_{DSS} with no RF signal applied. The source is grounded. Input power between 18 and 19 dBm.

I_{DSS}: Saturated drain-source current. Search for the maximum I_{DSS} at V_{GS} = 0.0 V, and V_{DS} swept between 0.5 V to 3.5 V. Note the drain voltage at which I_{DSS} is located and recorded as V_{DSP}.

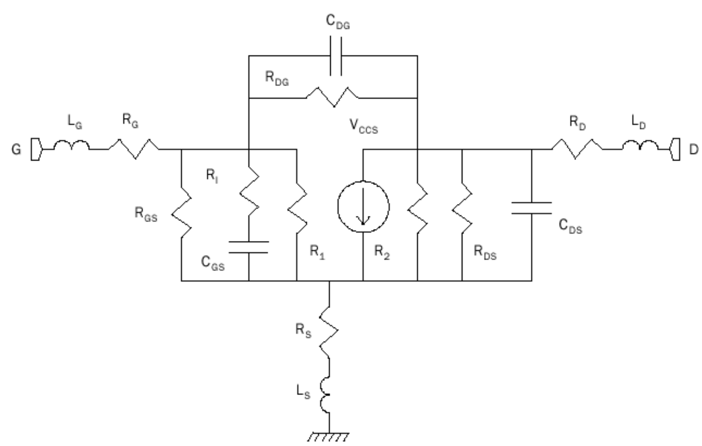
G_M: Transconductance. $(I_{DSS} – I_{DS1})/|V_{G1}|$. I_{DS1} measured at V_{G1} = -0.25 V using the knee search technique; V_{DS} swept between 0.5 V and V_{DSP} to search for maximum I_{DS1}.

V_P: Pinch off voltage. V_{GS} for I_{DS} =0.5 mA/mm of gate width. V_{DS} fixed at 2.0 V, V_{GS} swept to bring I_{DS} to 0.5 mA/mm. Sweep will stop if V_P current is not found beyond 0.5 V of the minimum V_P specification.

BV_{GS}: Breakdown voltage, gate to source. I_{BD} = 1.0 mA/mm of gate width. Source fixed at ground, drain not connected (floating). When 1.0 mA/mm is drawn at gate, V_{GS} measured as BV_{GS}.

BV_{GD}: Breakdown voltage, gate to drain. I_{BD} = 1.0 mA/mm of gate width. Drain fixed at ground, source not connected (floating). When 1.0 mA/mm is drawn at gate, V_{GD} measured as BV_{GD}.

LINEAR MODEL



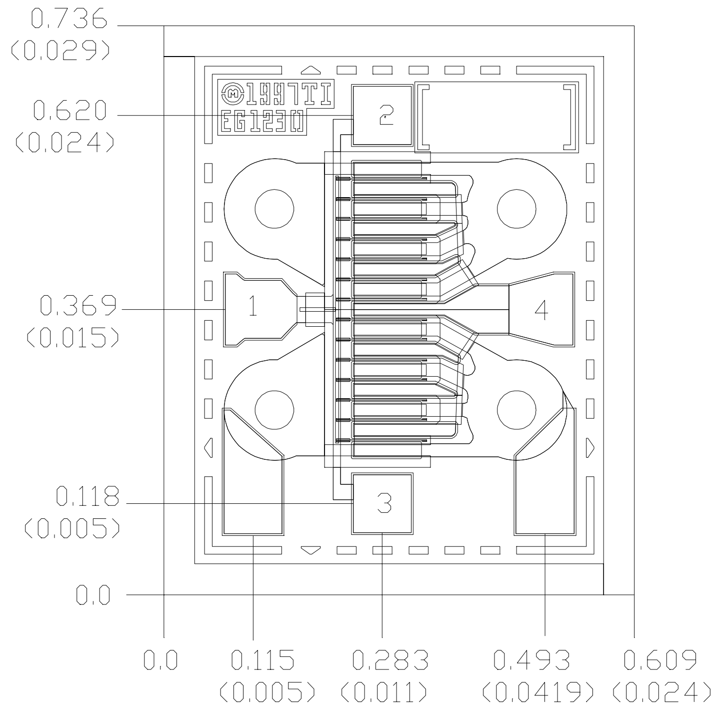
V_{DS} = 8.0 V and 30% I_{DSS} at T = 25°C

FET Elements	R_{DG} = 204000 Ω	**VCCS Parameters**
L_G = 0.0421nH	R_S = 0.4 Ω	M = 132.9 mS
R_G = 0.43 Ω	L_S = 0.015 nH	A = 0
R_{GS} = 81700 Ω	R_{DS} = 98.01 Ω	R1 = 1E19 Ω
R_I = 1.21Ω	C_{DS} = 0.25325 pF	R2 = 1E19 Ω
C_{GS} = 1.21 pF	R_D = 0.66 Ω	F = 0
C_{DG} = 0.1004 pF	L_D = 0.022 nH	T = 5.49 pS

MODELED S-PARAMETERS

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)
0.5	0.985	-29.88	8.095	161.49	0.021	72.66	0.343	-22.22
1.0	0.959	-56.20	7.297	145.18	0.038	58.80	0.328	-41.75
1.5	0.931	-77.47	6.368	131.86	0.050	47.65	0.312	-57.46
2.0	0.908	-94.02	5.512	121.22	0.057	39.12	0.301	-69.57
2.5	0.891	-106.82	4.791	112.62	0.062	32.60	0.295	-78.80
3.0	0.880	-116.82	4.202	105.49	0.065	27.55	0.294	-85.89
3.5	0.871	-124.76	3.723	99.42	0.067	23.56	0.297	-91.41
4.0	0.865	-131.19	3.330	94.11	0.068	20.34	0.302	-95.80
4.5	0.861	-136.48	3.004	89.37	0.069	17.70	0.309	-99.38
5.0	0.858	-140.92	2.732	85.06	0.069	15.51	0.319	-102.37
5.5	0.856	-144.69	2.501	81.09	0.069	13.67	0.329	-104.94
6.0	0.855	-147.94	2.304	77.39	0.068	12.12	0.340	-107.18
6.5	0.854	-150.78	2.133	73.90	0.068	10.82	0.352	-109.19
7.0	0.854	-153.29	1.984	70.59	0.067	9.72	0.364	-111.03
7.5	0.854	-155.53	1.852	67.43	0.066	8.80	0.377	-112.73
8.0	0.855	-157.54	1.736	64.40	0.065	8.05	0.390	-114.32
8.5	0.855	-159.37	1.632	61.49	0.065	7.45	0.404	-115.84
9.0	0.856	-161.04	1.539	58.67	0.064	7.00	0.417	-117.29
9.5	0.857	-162.58	1.455	55.95	0.063	6.68	0.430	-118.68
10.0	0.858	-164.01	1.378	53.30	0.061	6.49	0.444	-120.03
10.5	0.859	-165.34	1.308	50.73	0.060	6.43	0.457	-121.35
11.0	0.860	-166.58	1.244	48.23	0.059	6.51	0.470	-122.63
11.5	0.862	-167.76	1.186	45.79	0.058	6.71	0.483	-123.89
12.0	0.863	-168.87	1.131	43.41	0.057	7.05	0.496	-125.11
12.5	0.864	-169.93	1.081	41.09	0.056	7.52	0.509	-126.32
13.0	0.866	-170.94	1.034	38.83	0.055	8.12	0.521	-127.51
13.5	0.867	-171.91	0.991	36.62	0.053	8.86	0.534	-128.68
14.0	0.869	-172.84	0.950	34.46	0.052	9.74	0.546	-129.82

V_{DS} = 8.0 V and 30% I_{DSS} at T = 25°C



Units: millimeters (inches)
Thickness: 0.102 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

Bond pad #1 (gate)	0.072 x 0.075	(0.003 x 0.003)
Bond pad #2 (gate)*	0.075 x 0.075	(0.003 x 0.003)
Bond pad #3 (gate)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #4 (drain)	0.083 x 0.077	(0.003 x 0.003)

Minimum connections to Bond pads 1 and 4. Sources are connected to backside metalization.

*Alternate gate pads used for paralleling TGF4230s or for multiple gate wires.

NOTES

Gate bias supplies should be designed to sink or source gate current. The magnitude and direction of the gate current is a function of bias point, load impedance, and drive level.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handing, assembly and test.