
HD66137T

High-Voltage Durable 240-Channel Common Driver
for Dot-Matrix STN LCD

HITACHI

ADE-207-291(Z)

Rev. 2

Aug. 03, 1999

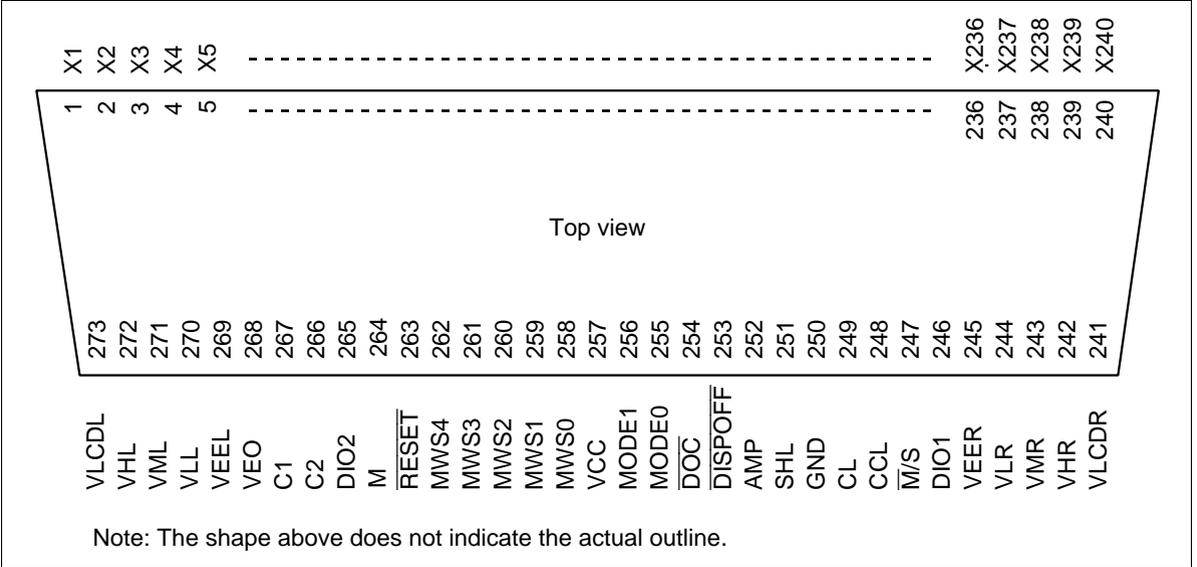
Description

The HD 66137T is a 240-channel common driver which drives a dot matrix STN LCD panel. By changing the mode, this can be applied to 240- and 200- and 160- channel output. Through the use of a 43-V high-voltage CMOS process technology, a high-voltage drive of +21.5 V and -21.5 V, centering on VM is possible. -21.5V generated from +21.5 V with built-in switching circuit and external capacity. Low logic-drive voltage (3 V) is used. This device is used together with the segment driver HD66130, HD66134ST or HD66136.

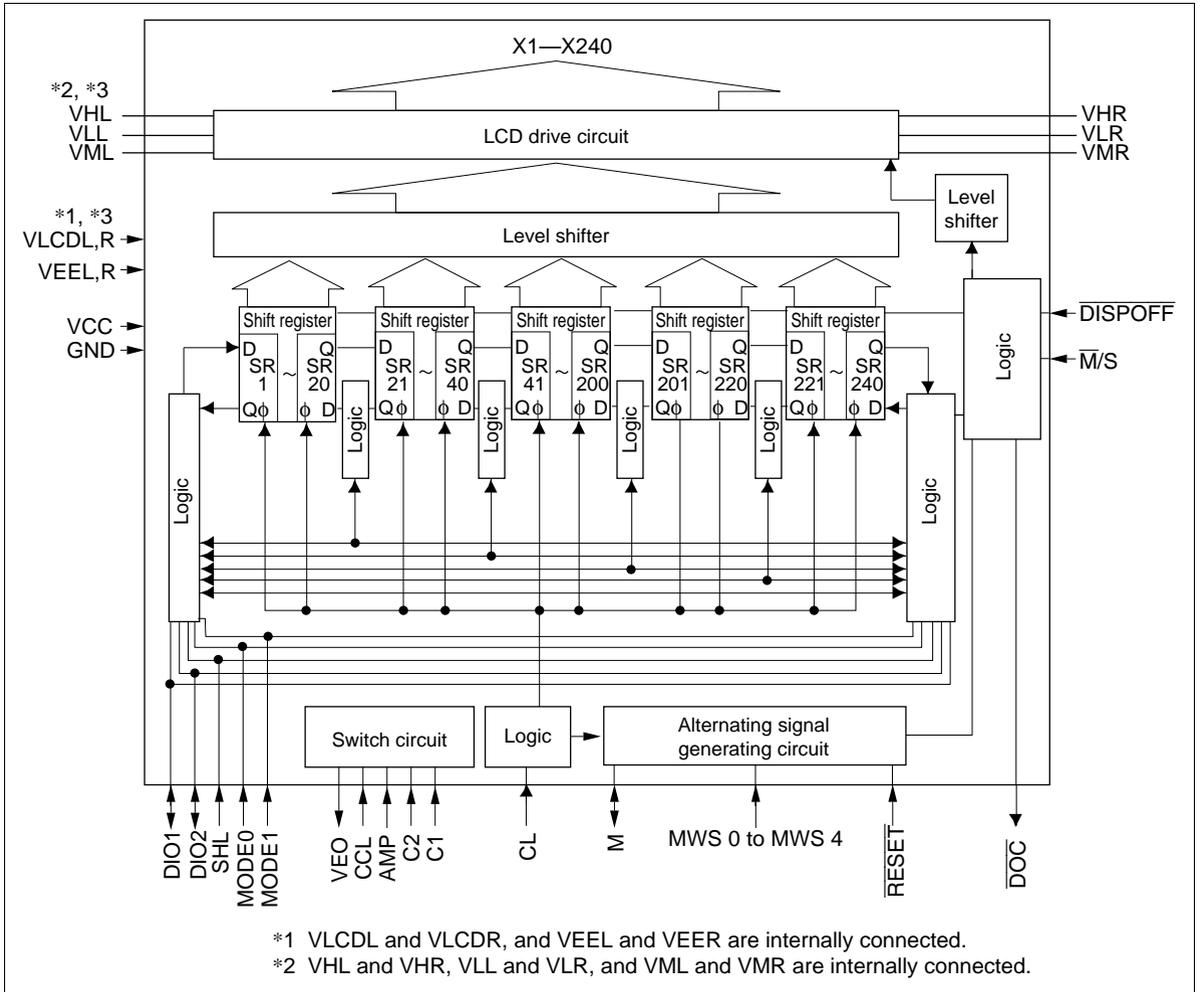
Features

- Display duty: Up to 1/240
- LCD drive voltage: 43 V max
- Built-in switching circuit (to generate -21.5 V)
- Number of LCD drive circuit: 240
- Operating voltage: 2.5 to 5.5 V
- Intermediate voltage I/F
- Built-in alternating signal generation circuit Pin programmable
- Output mode change: 240-output mode
200-output mode
160-output mode
- Built-in display-off function
- Flex TCP

Pin Arrangement



Block Diagram



Internal Block Diagram

1. LCD drive Circuit

This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.

2. Level shifter

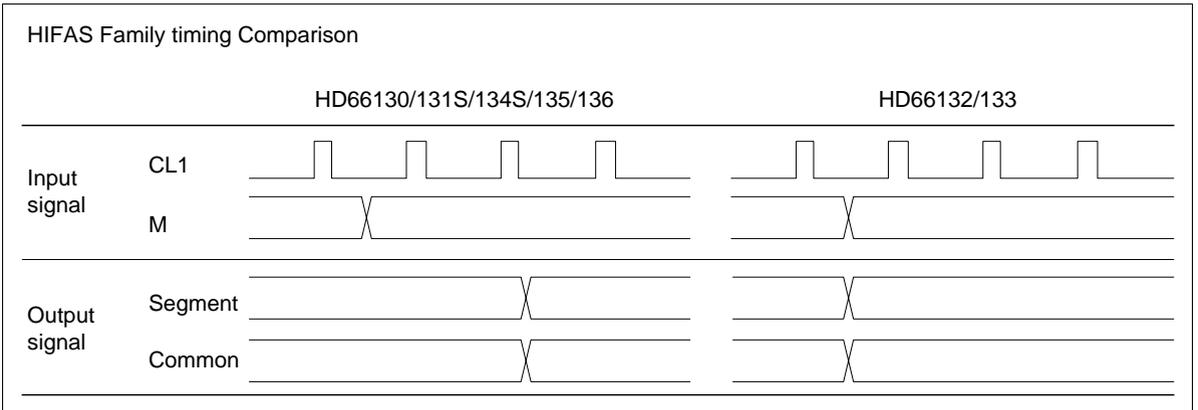
This boosts a 5-V signal to a high-voltage signal for LCD drive.

3. Shift register

This is a 240-bit bidirectional shift register circuit. The first line marker signal output from the DIO1 pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin.

4. Alternating signal generating circuit

This circuit generates an alternating signal (M signal) for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to V_{CC} or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins (MWS0 to MWS4) are connected to GND.



Pin Function

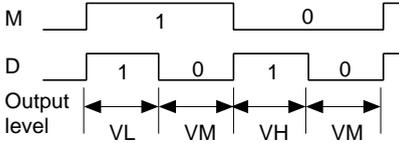
Classification	Symbol	Pin No.	Connected to	I/O	Functions																																																								
Power supply	VLCDL, R	273, 241	Power supply	—	VLCDL, R–VEEL, R : Power supply for LCD drive VLCDL, R : Power supply for switch circuit V _{CC} –GND : Power supply for logic circuit																																																								
	VEEL, R	269, 245																																																											
	V _{CC}	257																																																											
	GND	250																																																											
	VHL, R	272, 242	Power supply	Input	Power supply for LCD drive level VHL, R : Selected level (Set to the same voltage as VLCDL, R.) VLL, R : Selected level (Set to the same voltage as VEEL, R.) VML, R : Non-selected level and Power supply for switch circuit																																																								
	VLL, R	270, 244																																																											
	VML, R	271, 243																																																											
	VEO	268	VEEL, R	output	When use built -in switching circuit and generate VEE, VEO pin connect to VEEL, R pins. VM voltage is point of reference and reversed and output the voltage input to the voltage between VLCD and VM. If built-in switching circuit is not used, don't connect any lines to this pin.																																																								
	C1, C2	267, 266	Capacitance	—	External capacitance should be connected here when using the switch circuit for generate VEE. If built-in switching circuit is not used, don't connect any lines to this pin.																																																								
Control signal	CL	249	MPU	Input	Shift clock input. Data is shifted at the falling edge of shift clock CL of the shift register.																																																								
	M	264	Extension driver or MPU	I/O	Inputs or outputs the alternating current for LCD drive output.																																																								
	MWS0	258	—	Input	This pin specifies the cycle of the alternating signal (M signal) in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the HD66131T is driven by an external alternating signal, specify the number of lines as zero.																																																								
	MWS1	259																																																											
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	MWS3	261																																																											
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Pin Functions (cont)

Classification	Symbol	Pin No.	Connected to	I/O	Function															
Control signal	MODE0	256	—	Input	Switch terminals for the number of LCD drive output pins.															
	MODE1	256																		
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DIO1	246	Extension driver or MPU	I/O	Serial data input output pin																
DIO2	265																			
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"H" level	serial output pin	serial input pin																		
"L" level	serial input pin	serial output pin																		
CCL	248	MPU	Input	Built-in switching circuit clock input. When use built-in switching circuit and generate V_{EE} , this pin connect CL pin. If built-in switching circuit is not used, CCL must be fixed to GND																
AMP	252	—	Input	Built-in swiching circuit on-off control. When use built-in switching circuit, this pin must be fixed to V_{CC} . If built-in switching circuit is not used, this pin must be fixed to GND																
$\overline{\text{RESET}}$	263	MPU or V_{CC}	Input	Setting this pin to GND sets initializes the alternating signal (M signal) circuit. A V_{CC} level RESET is normally used.																
$\overline{\text{DISPOFF}}$	253	MPU	Input	Setting this pin to GND sets LCD drive output X1 to X240 to the VM level.																
$\overline{\text{M/S}}$	247	—	Input	Controls the display-off function, and display-off signal output from $\overline{\text{DOC}}$ pin.																
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$\overline{\text{DOC}}$	254	—	Output	<table border="1"> <thead> <tr> <th>$\overline{\text{M/S}}$</th> <th>$\overline{\text{DOC}}$</th> </tr> </thead> <tbody> <tr> <td>"H" level</td> <td>When $\overline{\text{DISPOFF}}$ is Low level, output low level When $\overline{\text{DISPOFF}}$ is High level, output High level</td> </tr> <tr> <td>"L" level</td> <td>Until serial data input 16 times output low level from $\overline{\text{DOC}}$ pin</td> </tr> </tbody> </table>		$\overline{\text{M/S}}$	$\overline{\text{DOC}}$	"H" level	When $\overline{\text{DISPOFF}}$ is Low level, output low level When $\overline{\text{DISPOFF}}$ is High level, output High level	"L" level	Until serial data input 16 times output low level from $\overline{\text{DOC}}$ pin									
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<p>The diagram shows three signals over time: DISPOFF, DIO1,2, and DOC. DISPOFF is a square wave that is high for most of the duration and low for a short period. DIO1,2 shows a sequence of 16 pulses, numbered 1 through 16. DOC is a square wave that is low during the first 16 pulses of DIO1,2 and high for the remainder of the time.</p>																				
When using $\overline{\text{M/S}}$ is low level, $\overline{\text{DOC}}$ pin should be connect to SEG LSI Dispoff control pin.																				

Pin Functions (cont)

Classification	Symbol	Pin No.	Connected to	I/O	Function																																				
Control signal	SHL	251	—	Input	This pin switches shift directions. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SHL</th> <th>MODE0</th> <th>MODE1</th> <th>Shift direction</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td></td> <td></td> <td>Right shift</td> </tr> <tr> <td>level</td> <td>"H"</td> <td>"H"</td> <td>DIO2→SR1.....SR240→DIO1</td> </tr> <tr> <td></td> <td>"H"</td> <td>"L"</td> <td>DIO2→SR21.....SR220→DIO1</td> </tr> <tr> <td></td> <td>"L"</td> <td>"H"</td> <td>DIO2→SR41.....SR200→DIO1</td> </tr> <tr> <td>"L"</td> <td></td> <td></td> <td>Left shift</td> </tr> <tr> <td>level</td> <td>"H"</td> <td>"H"</td> <td>DIO1→SR240.....SR1→DIO2</td> </tr> <tr> <td></td> <td>"H"</td> <td>"L"</td> <td>DIO1→SR220.....SR21→DIO2</td> </tr> <tr> <td></td> <td>"L"</td> <td>"H"</td> <td>DIO1→SR200.....SR41→DIO2</td> </tr> </tbody> </table> <p>SR1, SR2...SR240 correspond to X1, X2...X240. Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non-selected level synchronized every time; release these pins.</p>	SHL	MODE0	MODE1	Shift direction	"H"			Right shift	level	"H"	"H"	DIO2→SR1.....SR240→DIO1		"H"	"L"	DIO2→SR21.....SR220→DIO1		"L"	"H"	DIO2→SR41.....SR200→DIO1	"L"			Left shift	level	"H"	"H"	DIO1→SR240.....SR1→DIO2		"H"	"L"	DIO1→SR220.....SR21→DIO2		"L"	"H"	DIO1→SR200.....SR41→DIO2
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	"L"	"H"	DIO1→SR200.....SR41→DIO2																																						

LCD drive output	X1 to X240	1 to 240	LCD	Output	LCD drive output By a combination of the display data and the M signal, when DISPOFF is set to V _{CC} , either VH, VL, or VM is selected and transmitted to the output circuit. 
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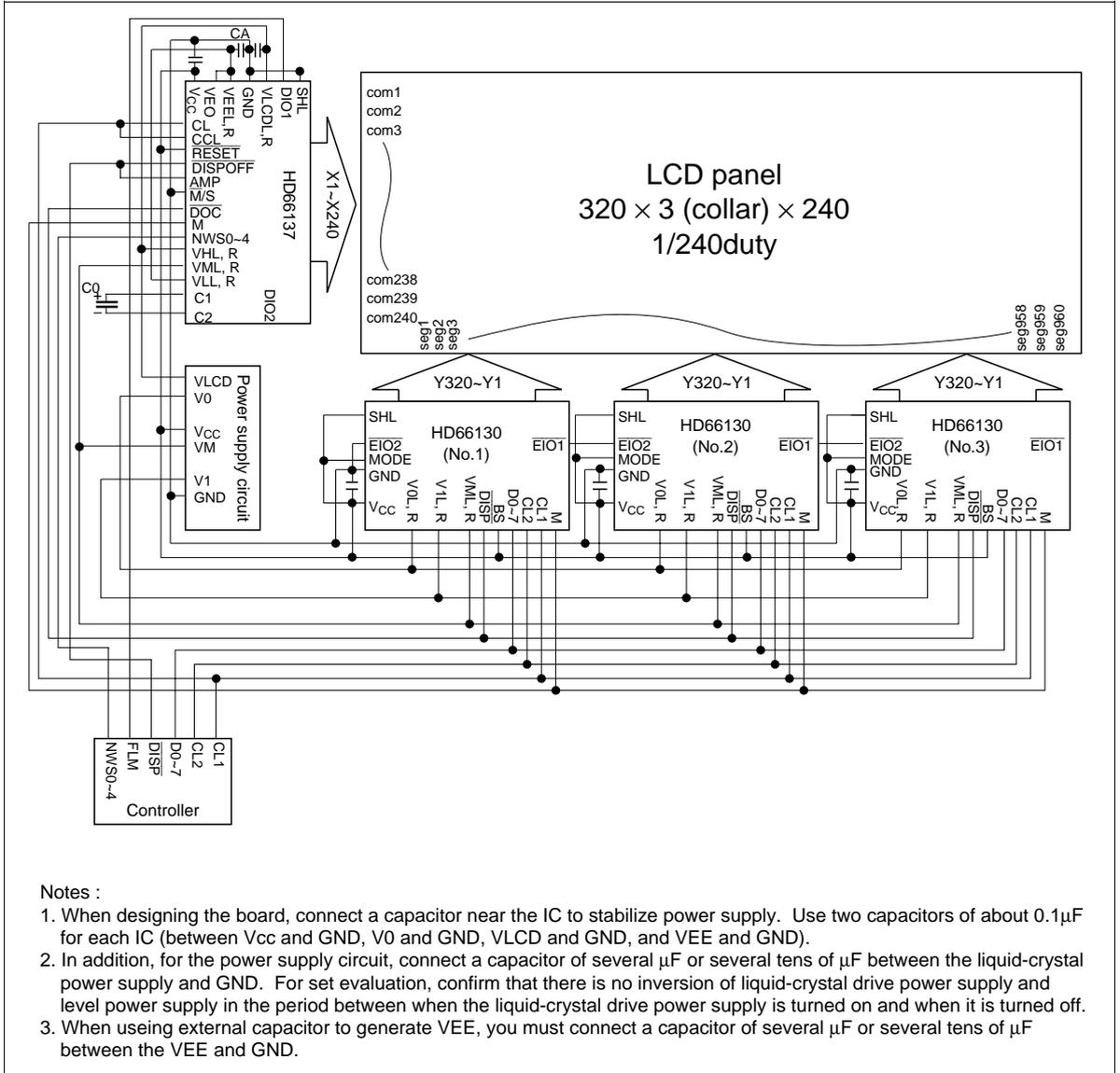
Note: Configuring the LCD panel using the HD66137 when using the select SEGMENT driver.

The Select SEGMENT driver

SEGMENT driver	Select
HD66130 (320 OUT)	○
HD66132 (240 OUT)	×
HD66134S (240 OUT)	○
HD66136 (400 OUT)	○

Application Example (2)

Figure 2 shows an application example 320 × 3 (collar) × 240 dot Quarter VGA Size STN color panel. This panel configured HD66137 × 1 piece and HD66130 × 3 pieces. HD66137 generates M signal and DOC signal. M signal pin is connected M signal pin of HD66130 and DOC signal pin is connected DISP signal pin of HD66136. HD66137 is able to generate - voltage by external capacitor. VEO pin is connected VEE pin and VL pin.



Notes :

1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1μF for each IC (between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND).
2. In addition, for the power supply circuit, connect a capacitor of several μF or several tens of μF between the liquid-crystal power supply and GND. For set evaluation, confirm that there is no inversion of liquid-crystal drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. When using external capacitor to generate VEE, you must connect a capacitor of several μF or several tens of μF between the VEE and GND.

Figure 2 Application Example (2)

Power Supply Circuit Example

Figure 3 shows a power supply circuit example.

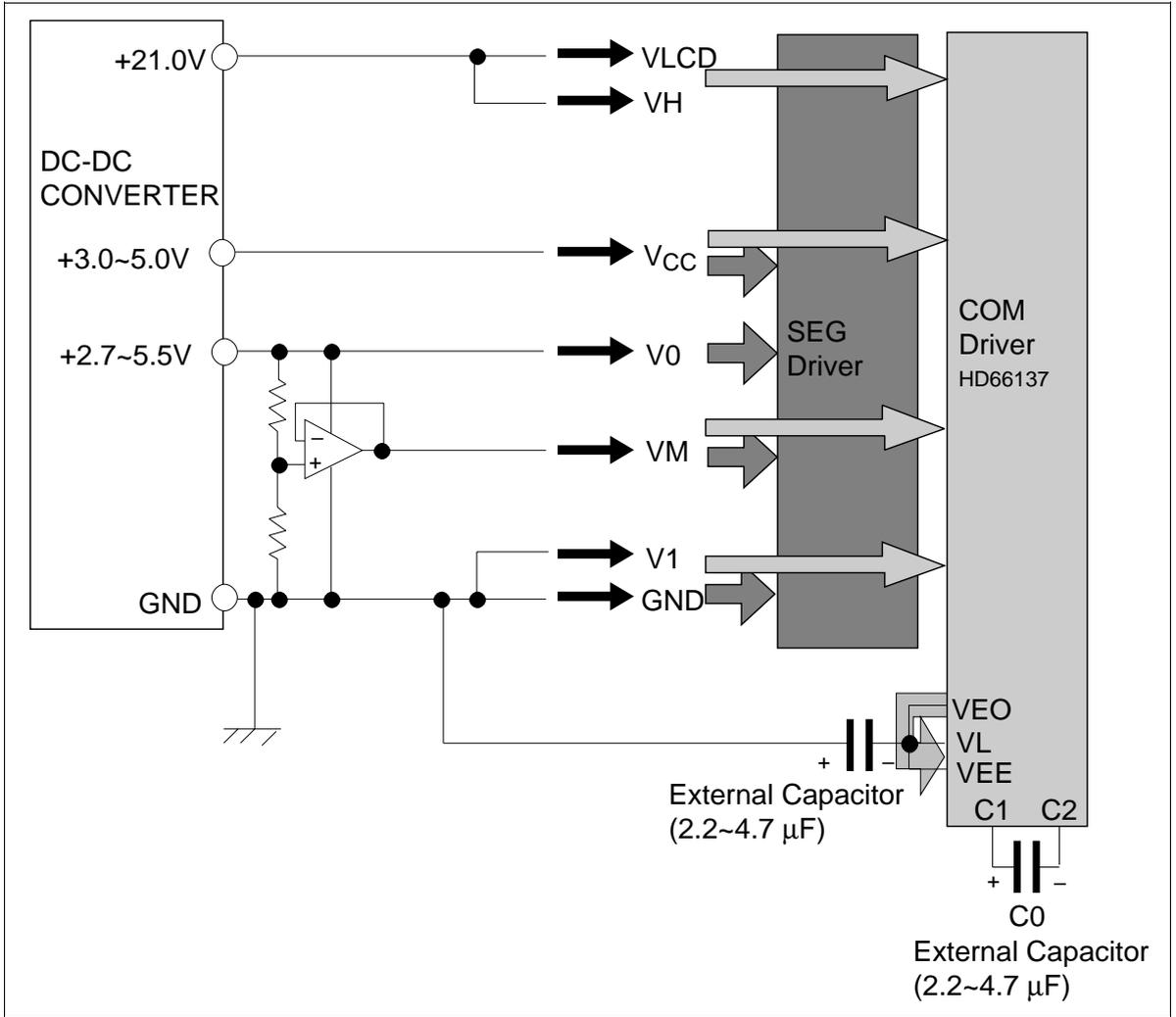


Figure 3 Power Supply Circuit Example

Absolute Maximum Rating

Item	Symbol	Ratings	Unit	Notes	
Power supply voltage	Logic circuit	V_{CC}	-0.3 to +7.0	V	1, 8
	LCD drive circuit	V_{LCD}	-0.3 to +25.0	V	1, 3, 8
		V_{EE}	-20.0 to +0.3	V	1, 4, 8
Input voltage (1)	VT1	-0.3 to $V_{CC} + 0.3$	V	1, 2	
Input voltage (2)	VH	-0.3 to V_{LCD}	V	1, 5, 8	
Input voltage (3)	VL	+0.3 to V_{EE}	V	1, 6, 8	
Input voltage (4)	VM	-0.3 to + 5.0	V	1, 7, 8	
Operating temperature	Topr	-30 to +75	°C		
Storage temperature	Tstg	-55 to +110	°C		

Notes: 1. Voltage from GND.

2. Applicable to DIO1, $\overline{DISPOFF}$, SHL, M, NWS0, NWS1, NWS2, NWS3, NWS4, \overline{RESET} , MODE0, MODE1, CL, $\overline{M/S}$, AMP, CCL, DIO2.

3. Applicable to V_{LCDL} , R pins.

4. Applicable to V_{EEL} , R pins.

5. Applicable to V_{HL} , R pins.

6. Applicable to V_{LL} , R pins.

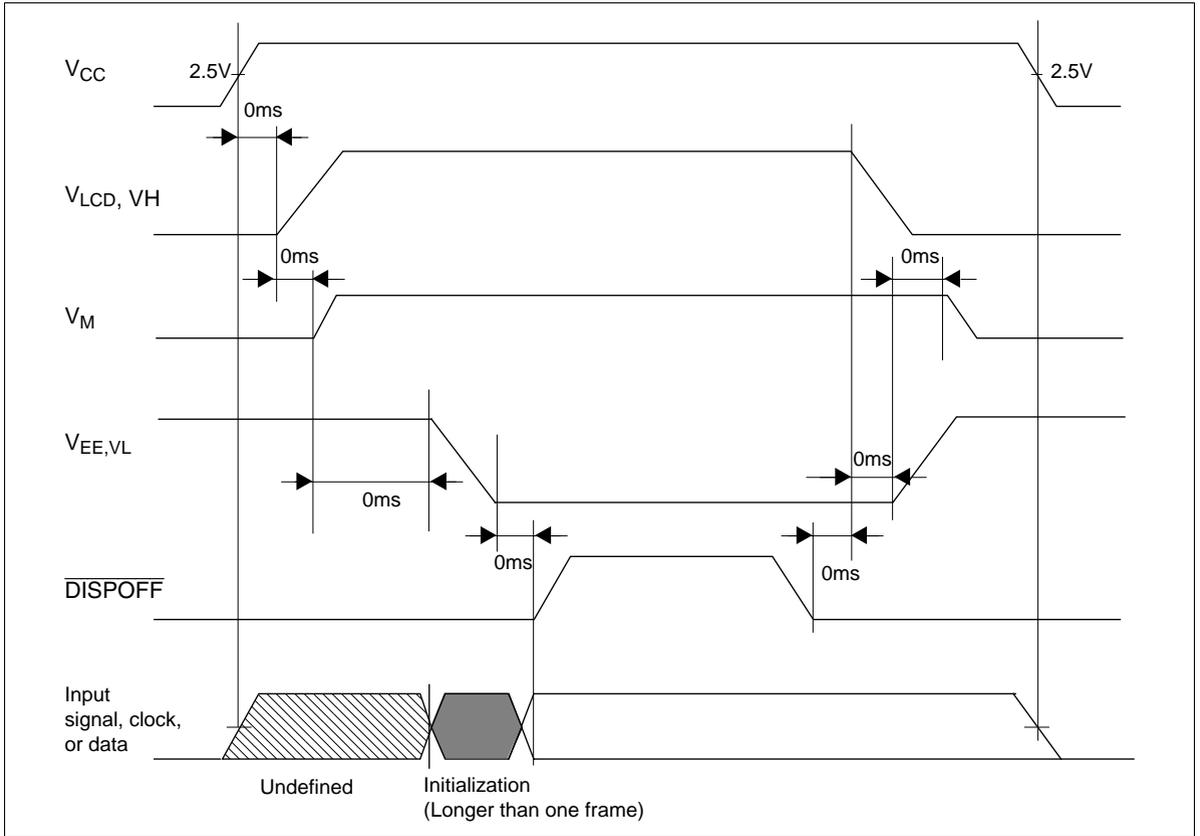
7. Applicable to V_{ML} , R pins.

(Caution)

Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.

8. Observe the sequence of activation and inactivation for the following power supplies and signals. And this sequence apply to use built - in switching circuit.

If the sequence is not observed, it may cause LSI malfunction, permanent damage, or adverse effects.



8.1 Power on

- (1) Turn on the power supply in the order of GND- V_{CC} , GND- V_{LCD} (VH), and VM. VM-VEE is generated automatically. In this case, input GND to the $\overline{DISPOFF}$ pin.
- (2) The LCD level forcibly outputs the VM level by the $\overline{DISPOFF}$ function.
- (3) The $\overline{DISPOFF}$ function has a priority even if input signal distortion occurs immediately after V_{CC} input.
- (4) Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.
- (5) Preparation for normal display is thus completed. Cancel the $\overline{DISPOFF}$ function by setting the $\overline{DISPOFF}$ pin to V_{CC} . At this point, the levels of VEE (VL), VLCD (VH) and VM must have reached the predetermined respective voltage.

8.2 Shut down

As a rule, shut down in order opposite to that used for power on.

- (1) Set the $\overline{DISPOFF}$ pin to GND.
- (2) At first shut off the LCD power supply GND- V_{LCD} (VH), at same time GND-VEE (VL) get to VM. Next shut off the VM.
- (3) Set V_{CC} and the input signal to GND.
At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0 V.
Since the $\overline{DISPOFF}$ function is inactivated when the V_{CC} level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.

Electrical Characteristics

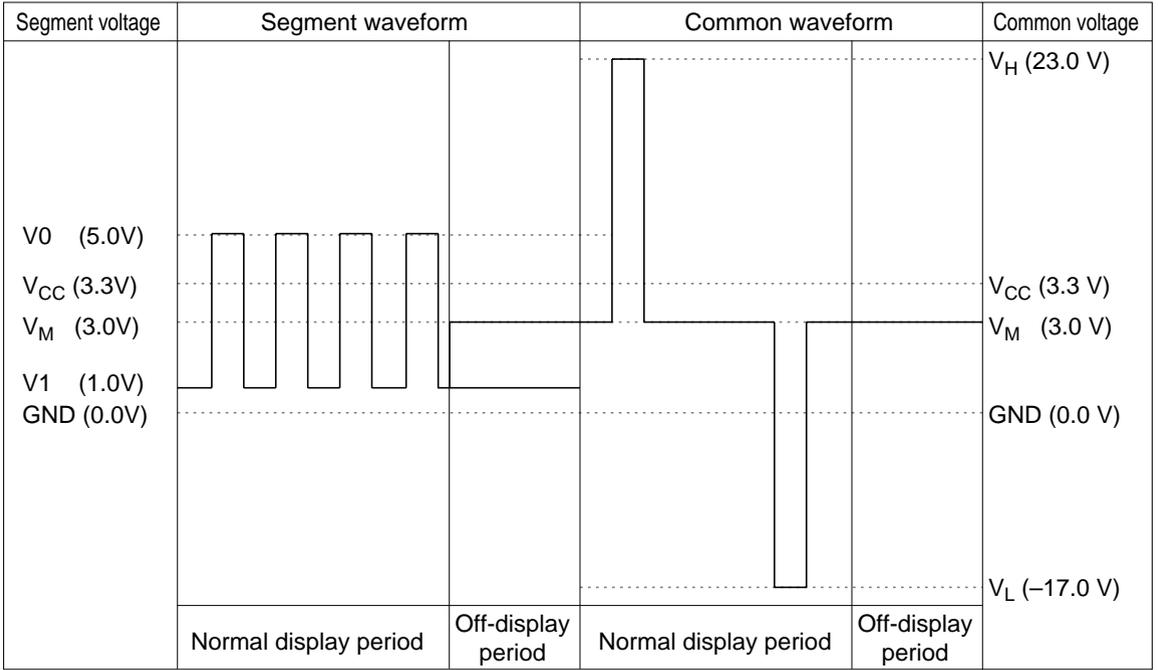
DC Characteristics ($V_{CC} = 2.5$ to 5.5 V, $GND = 0$ V, $V_{LCD} - V_{EE} = 15$ to 43 V, $T_a = -30$ to $+75$ °C)

Item	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit	Measurement Conditions	Notes
Input high-level voltage	V_{IH}	DIO1, $\overline{DISPOFF}$, SHL, M, $\overline{M/S}$, MWS0-4, \overline{RESET} ,	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low-level voltage	V_{IL}	CL, MODE0, MODE1, \overline{DOC} , AMP, CCL, DIO2	0	—	$0.3 \times V_{CC}$	V		
Output high-level voltage	V_{OH}	M, \overline{DOC} , DIO1, DIO2	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4$ mA	
Output low-level voltage	V_{OL}	M, \overline{DOC} , DIO1, DIO2	—	—	0.4	V	$I_{OL} = 0.4$ mA	
ON resistance between $V_i - Y_j$	R_{ON}	X1 to X240, V pin	—	0.7	2.0	k Ω	$I_{ON} = 150$ μ A	1
Input leak current (1)	I_{IL1}	DIO1, $\overline{DISPOFF}$, SHL, M, $\overline{M/S}$, MWS0-4, \overline{RESET} , CL, MODE0, MODE1, \overline{DOC} , AMP, CCL, DIO2	-5	—	5	μ A	$V_{IN} = V_{CC}$ to GND	
Input leak current (2)	I_{IL2}	VH, VL, VM, C1, C2	-25	—	25	μ A		
Current consumption (1)	I_{CC1}	V_{CC}	—	10	40	μ A	$V_{CC} = 3.3$ V, $V_{LCD} - V_{EE} = 40$ V, $f_{CL} = 19.2$ kHz, $f_M = 1.5$ kHz	2
Current consumption (2)	I_{CC2}	V_{CC}	—	20	50	μ A	$V_{CC} = 5.0$ V, $V_{LCD} - V_{EE} = 40$ V, $f_{CL} = 19.2$ kHz, $f_M = 1.5$ kHz	
Current consumption (3)	I_{LCD}	V_{LCD}	—	25	50	μ A	$V_{CC} = 3.3$ V, $V_{LCD} - V_{EE} = 40$ V, $f_{CL} = 19.2$ kHz, $f_M = 1.5$ kHz	

Notes: 1. This is a resistance value between the X and V pins (either of VH, VL, or VM) when a load current is applied to one of x1 to x240 pins. These values are regulated under the conditions of $V_{LCD} = V_H = 21.75$ V, $V_{EE} = V_L = -18.5$ V, $V_M = 1.75$ V, $GND = 0$ V, Use VH, VL, and VM in the range of $V_{LCD} - V_M \geq V_H - V_M = 21.5$ to 7.5 V, $V_{EE} - V_M \leq V_L - V_M = -21.5$ to -7.5 V, with the relation of $V_H > V_M > V_L$.

2. The current applied between the input and output is excluded. When an input to a CMOS gate is at an intermediate level, through current flows between the power supplies, and the power supply current increases. Therefore, use $V_{IH} = V_{CC}$ and $V_{IL} = GND$.

3. The voltage relationship of each signal is as follows :



AC Characteristics (1) ($V_{CC} = 2.5$ to 5.5 V, $GND = 0$ V, $V_{LCD} - V_{EE} = 15$ to 43 V, $T_a = -30$ to $+75$ °C)

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Clock cycle time	t_{CYC}	CL	400	—	ns	
CL high-level width	t_{CWH}	CL	25	—	ns	
CL low-level width	t_{CWL}	CL	370	—	ns	
CL rising time	t_r	CL	—	30	ns	
CL falling time	t_f	CL	—	30	ns	
Data set-up time	t_{DS}	DIO1, DIO2, CL	100	—	ns	
Data hold time	t_{DH}	DIO1, DIO2, CL	10	—	ns	
Data output delay time	t_{DD}	DIO1, DIO2, CL	—	200	ns	1
M output delay time	t_{MD}	M, CL	—	200	ns	1
M set-up time	t_{MS}	M, CL	20	—	ns	
M Hold time	t_{MH}	M, CL	20	—	ns	
DOC delay time 1	t_{DOC1}	$\overline{DISPOFF}$, \overline{DOC}	—	300	ns	2
DOC delay time 2	t_{DOC2}	DIO1, DIO2, \overline{DOC}	—	300	ns	2

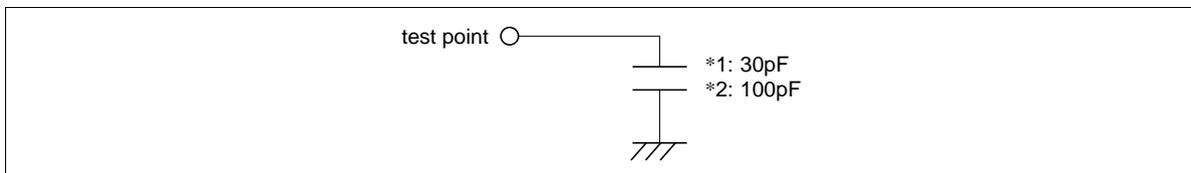
AC Characteristics (2) ($V_{CC} = 2.5$ to 4.5 V, $GND = 0$ V, $V_{LCD} - V_{EE} = 43$ V, $T_a = -30$ to $+75$ °C)

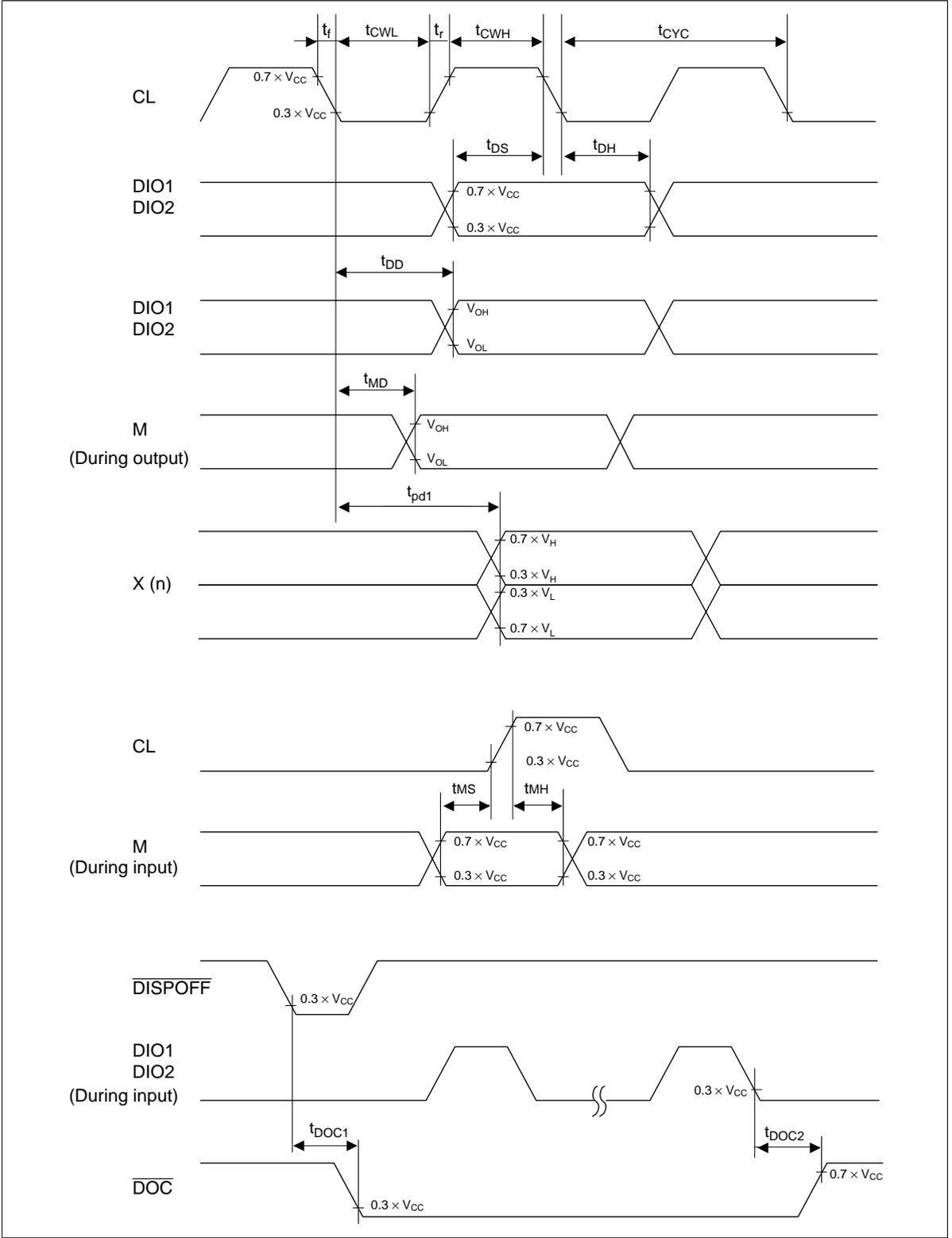
Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Output delay time1	t_{pd1}	X(n), M	—	1.2	μ s	2

AC Characteristics (3) ($V_{CC} = 4.5$ to 5.5 V, $GND = 0$ V, $V_{LCD} - V_{EE} = 43$ V, $T_a = -30$ to $+75$ °C)

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Output delay time1	t_{pd1}	X(n), M	—	0.7	μ s	2

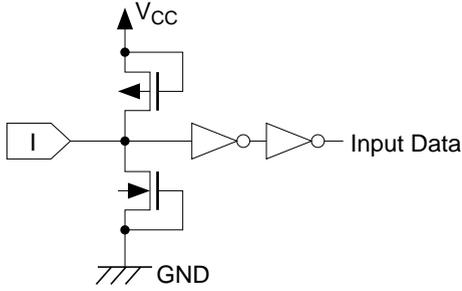
*1, *2. The following timing is regulated with the circuit at the right connected.



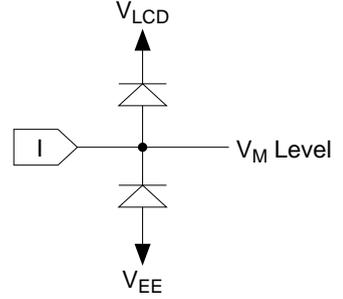


Terminal Configuration

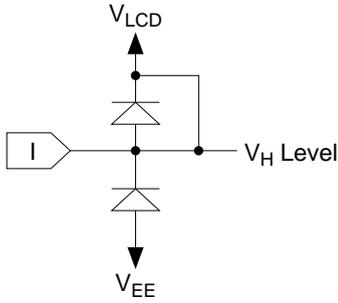
Terminal Configuration (1)



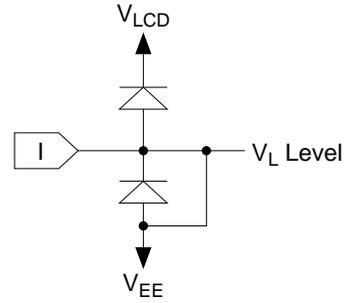
Input Terminal 1
 Applicable terminals :
 CL, CCL, SHL, MODE0,1, AMP
 DISPOFF, RESET, MWS0~4, M/S



Input Terminal 2
 Applicable terminals : $V_{MR, L}$
 * V_{MR} terminal connect with V_{ML} terminal in LSI.



Input Terminal 3
 Applicable terminals : $V_{HR, L}$
 * V_{HR} terminal connect with V_{HL} terminal in LSI.

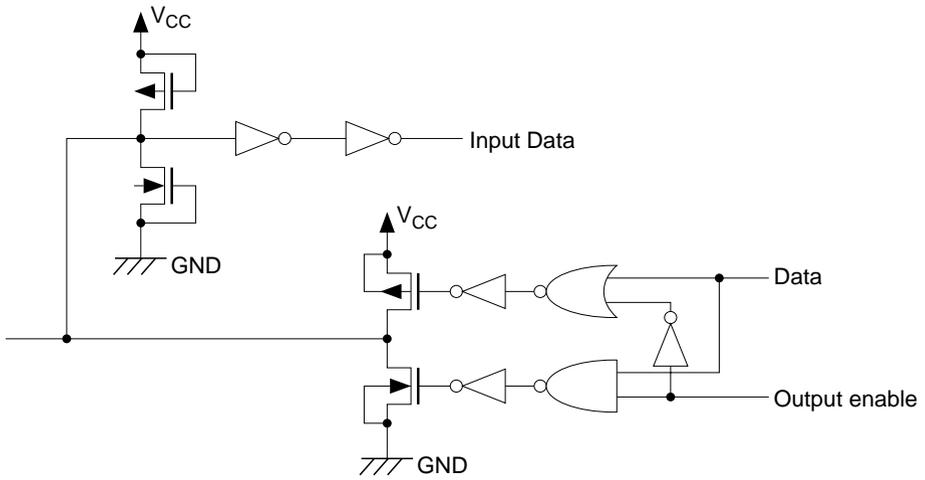


Input Terminal 4
 Applicable terminals : $V_{LR, L}$
 * V_{LR} terminal connect with V_{LL} terminal in SLI.

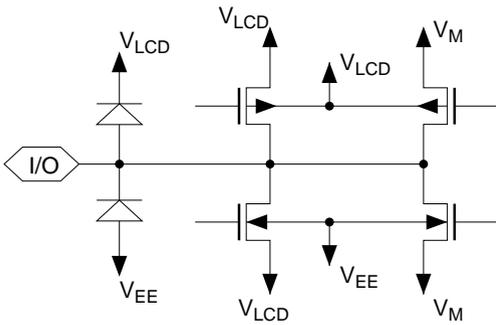


Output Terminal 1
 Applicable terminals : \overline{DOC}

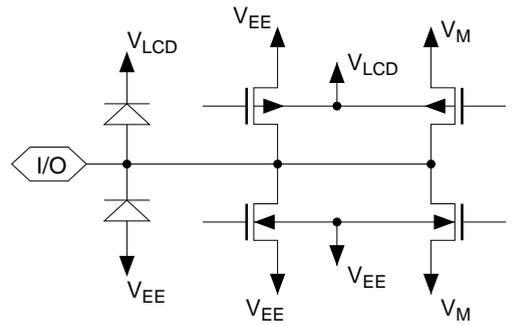
Terminal Configuration (2)



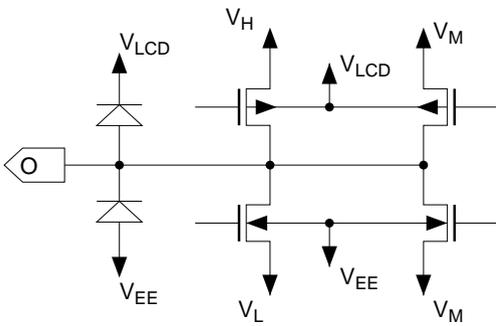
I/O Terminal 1
Applicable terminals : DIO1, DIO2, M,



I/O Terminal 2
Applicable terminals : C1



I/O Terminal 3
Applicable terminals : C2



LCD drive Output Terminal
Applicable terminals : X1 to X240

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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