NEC Electronics Inc.

CB-C9
3.3-Volt, 0.35-Micron Cell-Based CMOS ASIC

Preliminary

June 1996

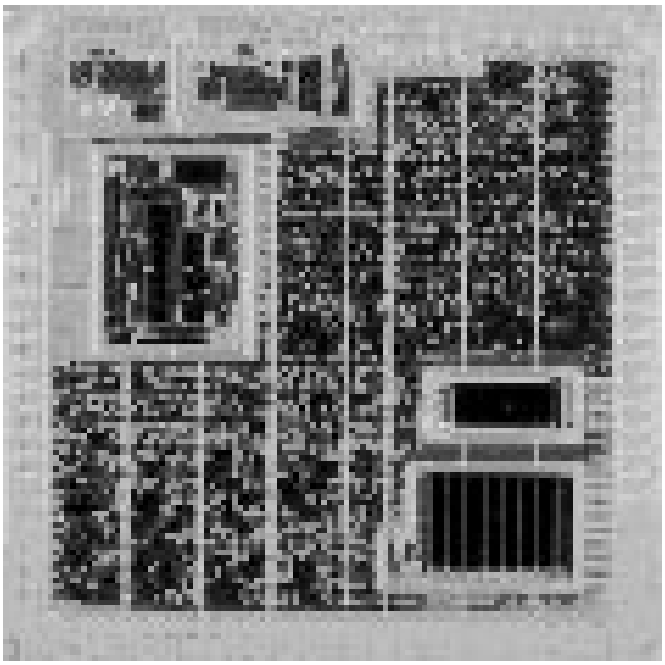
Description

NEC's CB-C9 CMOS cell-based ASIC family facilitates the design of complete cell-based silicon systems composed of user-defined logic, complex macro-functions such as microprocessors, intelligent peripherals, analog functions, and compiled memory blocks.

The CB-C9 cell-based ASIC series employs a 0.35-micron (0.27-micron effective) silicon gate CMOS process with silicidation. This advanced process greatly reduces the number of contacts per cell, leading to area-efficient library elements optimized on speed with a 3.3-V power supply. CB-C9 achieves 1.6M usable gates. A library option for 2.5-V power supply voltage is being developed. For this technology, the Titanium-Silicide process results in up to 30% reduced power consumption per cell, compared to 0.5-micron 3.3-V technologies. Combining very high integration, super high-speed, and low power consumption, this technology meets today's high-performance application demands.

Fully supported by NEC's sophisticated OpenCAD® design framework, CB-C9 maximizes design quality and flexibility while minimizing ASIC design time.

Figure 1. System-on-Silicon



NEC's OpenCAD system combines popular third-party design tools with proprietary NEC tools, including advanced floorplanner and clock tree synthesis tools.

Table 1. CB-C9 Family Features and Benefits

CB-C9 Family Features	CB-C9 Family Benefits
• 0.35-micron (drawn), Ti-Silicide CMOS technology	• High-density cell structure
• 3.3-V operation (2.5-V in development)	• Super high-speed at low power supply
• 26 base sizes, each with 2- and 3-metal layer options	• Flexible base sizes to best fit design needs
• Usable gates from 37K to 1.6M gates	• Super high integration capabilities
• Level shifter I/O: 3.3-V external to 2.5-V internal	• Supports flexible interfacing to different signal voltages
• Three pad ring options for high gate to pad ratio	• Minimizes device cost for high I/O requirement
• PCI buffer, including 66 MHz PCI	• PCI support compliant with latest PCI specification
• GTL, HSTL, pECL buffer support	• High-speed I/F to memory and processor buses
• Low power dissipation: 0.7 µW/MHz/gate (3.3-V), 0.5 µW/MHz/gate (2.5-V)	• Ideally-suited for hand-held applications
• Extensive macro selection (CPUs, peripherals, analog)	• Supports advanced system-on-silicon design
• Datapath compiler for various types of ALU, multiplier, adder	• Speed & area-effective memory modules
• Memory compiler for various types of memory blocks	• Area-effective memory integration on-chip
• Extensive package support: PQFP, BGA, TBGA, CSP	• Delivers the latest package requirements
• Automatic clock skew control by clock tree synthesis	• Minimizes on-chip clock skew
• Popular, third-party CAE tools	• Smooth design flow from customer design to silicon

5-V-Tolerant Interface

CB-C9 supports both 3.3-V and 5-V-tolerant signaling. The 5-V-tolerant buffers enable CB-C9 devices to communicate to 5-V TTL signal while protecting the ASIC. If 5-V-tolerant buffers are not required, 3.3-V buffers may be substituted, thus increasing the die area available for logic.

Integration and Performance

Gate complexities up to 1.6M usable gates can be integrated on the largest of 26 die sizes, each routable with 2- or 3-metal layers. This gives enough flexibility to optimally fit design needs. Three I/O ring options: a single I/O pad ring (type S); or two pitches of dual pad ring (types C and T). For details, please refer to Table 2.

Figure 2. CB-C9 5-V Interfacing

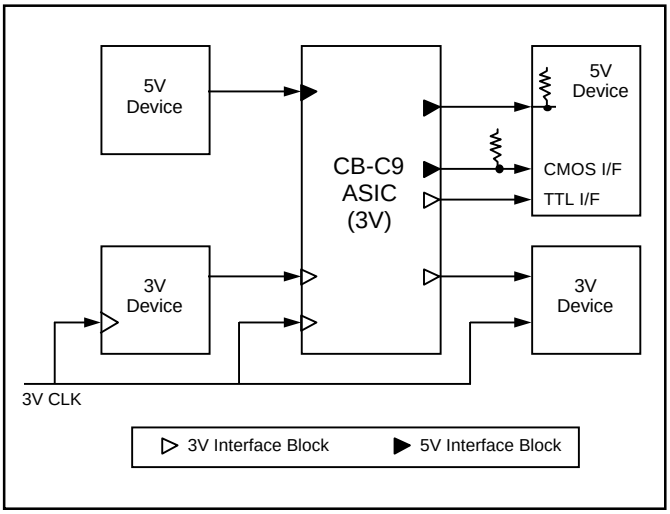


Table 2. CB-C9 Die Steps

Step Size	I/O Pitch (C)	(T)	(S)	Usable Gates (2LM) 3V I/O	3/5V I/O[1]	5V I/O	Usable Gates (3LM) 3V I/O	3/5V I/O[1]	5V I/O
B60C/T/S	196	156	108	49.9	37.1+3.2N	37.1	76.0	56.4+4.9N	56.4
C02C/T/S	236	180	128	64.4	50.0+3.6N	50.0	99.5	77.2+5.6N	77.2
C40C/T/S	268	204	144	82.2	65.8+4.1N	65.8	125.2	100.3+6.2N	100.3
C78C/T/S	300	223	160	99.4	81.5+4.5N	81.5	150.2	123.2+6.8N	123.2
D01C/T/S	316	244	168	109.5	90.9+4.7N	90.9	166.9	138.5+7.1N	138.5
D26C/T/S	336	256	178	123.4	103.5+5.0N	103.5	185.1	155.3+7.4N	155.3
D52C/T/S	356	276	188	139.3	118.2+5.2N	118.2	209.0	177.3+7.9N	177.3
D90C/T/S	388	300	204	159.7	137.3+5.6N	137.3	237.6	204.2+8.3N	204.2
E16C/T/S	408	312	214	176.6	152.9+5.9N	152.9	262.7	227.5+8.8N	227.5
E54C/T/S	444	340	232	198.9	174.1+6.2N	174.1	298.4	261.1+9.3N	261.1
E80C/T/S	464	352	242	218.0	191.9+6.5N	191.9	321.5	283.1+9.6N	283.1
F18C/T/S	500	380	260	240.9	213.8+6.8N	219.8	358.2	317.9+10.1N	317.9
F44C/T/S	516	396	268	261.3	232.4+7.2N	232.4	388.7	345.7+10.7N	345.7
F70C/T/S	540	412	280	282.0	252.6+7.3N	252.6	412.1	369.2+10.7N	369.2
G08C/T/S	568	432	294	306.9	275.9+7.7N	275.9	452.3	406.7+11.4N	406.7
G34C/T/S	596	452	308	328.8	297.4+7.8N	297.4	484.6	438.3+11.6N	438.3
G72C/T/S	624	472	322	364.0	331.0+8.3N	331.0	526.8	479.0+11.9N	479.0
H10C/T/S	656	496	338	390.1	356.3+8.5N	356.3	569.3	520.0+12.3N	520.0
H49C/T/S	692	524	350	426.5	391.1+8.8N	391.1	622.4	570.8+12.9N	570.8
H87C/T/S	720	544	370	466.6	428.7+9.5N	428.7	668.4	614.1+13.6N	614.1
J26C/T/S	752	568	386	492.4	454.9+9.4N	454.9	725.0	669.7+13.8N	669.7
J51C/T/S	772	588	396	620.0	480.5+9.9N	480.5	761.1	694.1+14.3N	694.1
K15C/T/S	824	624	422	591.9	549.6+10.6N	549.6	838.5	778.7+15.0N	778.7
K92C/T/S	892	676	456	660.9	617.9+10.7N	617.9	944.1	882.7+15.3N	882.7
M97C/T/S	1060	804	540	898.3	848.8+12.4N	848.8	1268.2	1198.2+17.5N	1198.2
P63C/T/S	1204	908	612	1102.9	1048.7+13.6N	1048.7	1537.4	1461.8+18.9N	1461.8

[1] N = The number of sides which are composed of only 3V I/F buffers

The family offers an extensive library of primitive macrofunctions characterized for 3.3-V operation (2.5-V operation in the future). Each of these blocks has several different drive strengths, allowing the synthesis tool to select the most suitable block for the required internal load. This generally reduces the design overhead without influencing design performance. The internal gate delay for a two-input NAND gate is 87 picoseconds (ps), (F/O=1, L=0mm, 3.3-V operation) and under loaded conditions 113 (F/O=2, L=typ, 3.3-V operation) and 120 ps (F/O=1, L=typ, 2.5-V operation).

To meet today's high-speed demands, high-performance I/O macros are mandatory. CB-C9 supports macros such as GTL, pECL, and HSTL for fast, low power data transfer, PLLs to synchronize on-chip system clocks, and PCI signaling standards. Also, CB-C9 offers a variety of macrofunctions to be incorporated on a single chip. These macrofunctions include CPU cores, peripheral devices, RAM/ROM, datapath macros and functions, enabling designers to perform system-on-silicon. Moreover, level shifters (connect between 3.3-V external and 2.5-V internal) are supported to provide low power consumption and flexible interfacing to different signal voltages making correspondence.

Low Power Consumption

NEC's CB-C9 Titanium-Silicide process features exceptionally low power dissipation to facilitate super high-speed operation without the need of costly package options. The process also drastically increases battery life for hand-held applications. The new ASIC family dissipates power at 0.7 µW/MHz/gate (3.3-V) and at 0.5 µW/MHz/gate (2.5-V).

Test Simplification Design

To test the logical circuit of 1.6M gate large-scale easily, CB-C9 allows use of Scan and Boundary Scan for logic area, BIST for memory macros, and direct accessed test bus architecture for core macros.

System on Silicon

NEC offers a wide selection of CPU/MCU cores, industry-standard intelligent peripheral macros, and compilable RAM/ROM blocks and datapath macros as well as analog functions in hard macro form that can be integrated onto a single CB-C9 chip. Including such macrofunctions in an ASIC design makes it possible to achieve a high level of integration, performance, and system security.

The range of NEC's proprietary 32-bit RISC CPUs include V810, V851 which has V810 core and 16-bit external data bus, and an upgraded high-speed version of the popular 16-bit CPU V30MX, which operates at clock speeds of 33 MHz at 3.3-V, and offers an improved 286-compatible address pipelining and uses a 24-bit address bus. Other specific cores can be implemented on request. For details about the full range of on-chip macrofunctions, refer to Table 3. Please also refer to Table 4 for compiled RAM specifications.

Embedded macrofunctions are easy to place, route, and simulate. Because these macros are derived from NEC's standard parts, they have fully characterized parameters and can be tested with standard test vectors to ensure full functionality and reliability.

NEC's test bus architecture allows complete system simulation, production testing of the internal circuits of the macrofunctions, and seamless embedded CPU core emulation. The CPU may be connected externally and can be replaced by an in-circuit emulator (ICE). All this is performed with only two dedicated test control pins.

CB-C9 Applications

Major advantages of NEC's CB-C9 ASIC family are high integration density, high speed and very low power consumption and cost-effective memory and megamacro integration.

Following these main advantages results in a wide range of applications. For example, high-performance transmission and switching systems, based on ATM technique, may take advantage from high speed, high integration density and high performance memory integration. High-end hand-held applications as PDA's or mobile communication equipment make use of low power and the capability of global system integration including powerful microprocessor cores, which results in small system cases. Future high-end consumer products such as digital TV set-top boxes need system-on-silicon integration to allow cost-effective mass production. High-end chipsets for engineering workstations (EWS) or graphic PC-subsystems need very high performance combined with cost-effective packaging solutions. With it's very low power consumption, NEC's CB-C9 family enables the usage of more cost-effective packaging solutions.

Table 3. CB-C9 Mega Macro Library (In Development)

	Macro	Comparable Device	Description
CPU	NZ70008H	Z80™	8-bit microprocessor
	NAV30MX	V30HL™	16-bit microprocessor
	NA70732	V810™	32-bit RISC microprocessor
	NAV851R48	V851™	32-bit RISC microprocessor
	ARM™	ARM7TDMI	32-bit RISC microprocessor
DSP		SPX	DSP
	OAK	OakDSPCore™	DSP
	OAK	PineDSPCore™	DSP
		MPEG2	MPEG2
		AC3 decoder	AC3 decoder
Peripheral	NA71037L	µPD71037	DMA controller
	NA71051L	µPD71051	USART, 30Kbit/s, full duplex
	NA71054L	µPD71054	Programmable timer/counter
	NA71055L	µPD71055	Programmable parallel interface
	NA71059L	µPD71059	Programmable interrupt controller
	NA4993AL	µPD4993	8-bit parallel I/O real-time clock
	NA72065VL	µPD72065B	Single- and double-density floppy disk controller
	NA16550L	NS16550A	UART with FIFO
Analog	—	—	8-bit 30 MHz ADC/DAC
	—	—	8-bit 220 MHz DAC
	—	—	8-bit 500 KHz ADC
	—	—	10-bit 100 KHz ADC
	—	—	10-bit 30 MHz DAC
	—	—	90 MHz Analog PLL
	—	—	150 MHz Analog PLL
	—	—	250 MHz Analog PLL
	—	—	RAC Rambus™ ASIC cell

Z80 is a trademark of Zilog, Incorporated
V30HL, V810, and V851 are trademarks of NEC Corporation
ARM is a trademark of Advanced RISC Machines
OakDSP Core is a trademark of DSP Group
PineDSP Core is a trademark of DSP Group
Rambus is a trademark of Rambus

Table 4. Compiled RAM Specification

RAM Type	3.3V Supply Voltage Tac[1] [ns]	3.3V Supply Voltage Pd[2] [mW/MHz]	2.5V Supply Voltage Tac[1] [ns]	2.5V Supply Voltage Pd[2] [mW/MHz]	Min. Size [bits x words]	Max. Size[3] [bits x words]
1-port high-speed	3.61	0.50	5.65	0.28	1 x 32	32 x 2048
1-port high-density	6.50	0.36	10.07	0.20	1 x 16	32 x 2048
1-port super high-speed	2.89	0.34[4]	—	—	1 x 64	16 x 1024
2-port high-speed	3.73	0.97	5.89	0.47	1 x 32	32 x 2048
2-port high-density	7.41	0.50	11.31	0.27	1 x 32	32 x 1024

(1) Max. access time at 8-bits x 512 words from clock to valid data with unloaded outputs
(2) Dynamic power dissipation
(3) Larger block sizes are available by connecting basic hard macros
(4) Additional DC power dissipation of 28 mW during read cycle

CAD Support

The CB-C9 family ASICs are completely supported by NEC's OpenCAD design environment, a unified front-to-back-end design package that allows designers to mix and match tools from the industry's most popular third-party vendors and from NEC's offering of powerful proprietary software tools. These tools perform schematic capture, logic synthesis, floorplanning, logic and timing simulation layout, design and circuit rule check, and memory compilation. The company's proprietary clock tree synthesis tool can be used to automatically buffer the clock lines as needed to minimize clock skew, essential for high-speed designs.

The library elements of NEC's CB-C9 family are modeled in a nonlinear way using table look-up methods. This allows the most accurate timing verification throughout synthesis, estimated timing simulation and sign-off timing simulation as it includes not only the influence of actual load conditions but also of the logic-cells input slopes. NEC developed this delay modeling method to enable a converging design flow and to minimize design iterations.

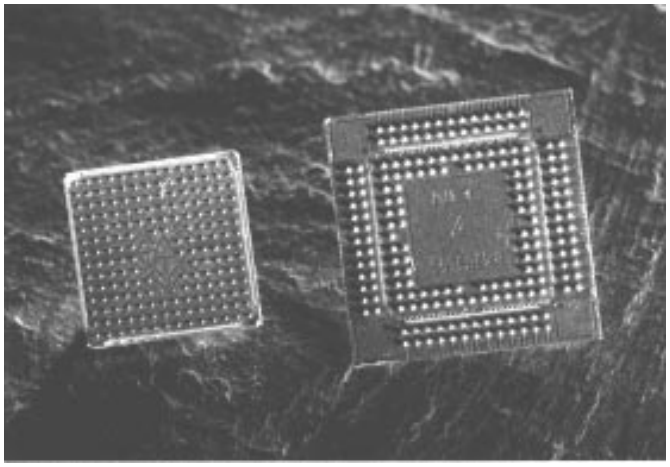
Test Support

The CB-C9 family supports automatic test generation through a scan test methodology, which allows higher fault coverage, easier testing and faster development time. This includes internal scan as well as boundary scan. NEC also offers optional built-in-self-test (BIST) architecture for RAM testing. Test of embedded megamacros is supported from NEC's test bus concept, which allows the use of predefined test pattern sets, for example, for integrated core macros.

Packaging

NEC offers a wide variety of over 60 package types. The CB-C9 family can be packaged in NEC's most popular surface-mount and through-hole packages. These include plastic quad flat packs (PQFPs) with optional heat spreader and pin counts in the range from 100 to 304 pins. Pin grid arrays (PGAs) with 364 or 528 pins and ball grid array (BGA) packages with 256 to 696 ball contacts are also supported. Also planned for release is the FBGA (CSP). See Figure 3 for package photo.

Figure 3. FBGA photo



Publications

This data sheet contains specifications, package information, and operational data for the CB-C9 cell-based family. Additional design information is available in NEC's *CB-C9 Block Library* and *CB-C9 Design Manual*. Call your local NEC ASIC design center representative or the NEC literature line for additional ASIC design information; see the back of this data sheet for locations and telephone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	–0.5 to +4.6V
I/O voltage, V_I	
3V input buffer (at $V_I < V_{DD}$ +0.5V)	–0.5 to +4.6V
3.3V fail-safe input buffer (at $V_I < V_{DD}$ +0.5V)	–0.5 to +4.6V
5V-tolerant buffer (at $V_I < V_{DD}$ +3.0V)	–0.5 to +6.6V
Output voltage, V_O	
3V buffer (at $V_O < V_{DD}$ +0.5V)	–0.5 to +4.6V
5V-tolerant buffer (at $V_O < V_{DD}$ +3.0V)	–0.5 to +6.6V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	–40 to +85°C
Storage temperature, T_{STG}	–65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance ($V_{DD} = V_I = 0V$; f = 1 MHz)

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

(1) Values include package pin capacitance

Power Consumption

Description	Limits	Unit
Internal cell (@ 3.3V supply voltage)	0.7	µW/MHz
Input block (FI01)	3.76	µW/MHz
Output block (FO02 @ 15 pF)	278	µW/MHz

(1) Assumes 30% internal gate switching at one time

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Recommended Operating Conditions (V_{DD} = 3.3V ± 0.3V; T_J = 0°C to +125°C)

Parameter	Symbol	3.3V Buffer Min	3.3V Buffer Max	5V-Tolerant Min	5V-Tolerant Max	3.3V PCI Min	3.3V PCI Max	Unit
I/O power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	3.0	3.6	V
Junction temperature	T_J	–0	+125	–0	+125	–0	+125	°C
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	V_{DD}	0.5 V_{DD}	V_{DD}+0.5	V
Low-level input voltage	V_{IL}	0	0.8	0	0.8	–0.5	0.3 V_{DD}	V
Input rise/fall time	t_R, t_F	0	200	0	200	0	200	ns
Input rise/fall time, Schmitt	t_R, t_F	0	10	0	10	0	200	ms

AC Characteristics (V_{DD} = 3.3V ± 0.3V; T_J = 0°C to +125°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	670			MHz	D-F/F; F/O = 1 mm
Delay time						
2-input NAND (F322)	t_{PD}		87		ps	F/O = 1; L = 0 mm
	t_{PD}		113		ps	F/O = 2; L = typ
Flip-flop (F611)	t_{PD}		488		ps	F/O = 1; L = 0 mm
	t_{PD}		514		ps	F/O = 2; L = typ
	t_{SETUP}	520			ps	—
	t_{HOLD}	200			ps	—
Input buffer (FI01)	t_{PD}		157		ps	F/O = 1; L = 0 mm
	t_{PD}		170		ps	F/O = 2; L = typ
Output buffer (12 mA) 3.3V	t_{PD}		675		ps	C_L = 0 pF
Output buffer (12 mA) 3.3V	t_{PD}		2375		ps	C_L = 50 pF
Output buffer (6 mA) 5V-tolerant	t_{PD}		1400		ps	C_L = 0 pF
Output buffer (6 mA) 5V-tolerant	t_{PD}		3650		ps	C_L = 50 pF
Output rise time (9 mA)	t_R		2.3		ns	C_L = 15 pF; 10-90%
Output fall time (9 mA)	t_F		1.8		ns	C_L = 15 pF; 10-90%

DC Characteristics (V_{DD} = 3.3V ± 0.3V; T_J = 0°C to +125°C)

Parameters	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Quiescent current						
H49 - P63	I_{DDS}	$V_I = V_{DD}$ or GND		40	TBD	µA
F18 - H10	I_{DDS}	$V_I = V_{DD}$ or GND		20	TBD	µA
B60 - E80	I_{DDS}	$V_I = V_{DD}$ or GND		10	TBD	µA
Off-state output leakage current						
3.3V output	I_{OZ}	$V_O = V_{DD}$ or GND			±10	µA
5V-tolerant	I_{OZ}	$V_O = V_{DD}$ or GND			±10	µA
Output sink current with pull-up (V_O = 3.3V)	I_R	V_{PU} = 5.5 V, R_{PU} = 2ký			TBD	µA
Output sink short circuit current	I_{OS}	V_O = GND			–250	mA
Input leakage current						
Regular	I_I	$V_I = V_{DD}$ or GND		$\pm 10^{-4}$	±10	µA
With pull-up resistor (50 kΩ)	I_I	V_I = GND	–36	–89	–165	µA
With pull-up resistor (5 kΩ)	I_I	V_I = GND	–284	–654	–1305	mA
With pull-down resistor (50 kΩ)	I_I	$V_I = V_{DD}$	28	79	141	µA
Pull-up resisor						
With pull-up resistor (50 kΩ)	R_{PU}		21.8	37.1	83.1	kΩ
With pull-up resistor (5 kΩ)	R_{PU}		2.8	5.0	10.6	kΩ
With pull-down resistor (50 kΩ)	R_{PD}		25.6	41.9	105.8	kΩ
Low-level output current						
3V buffers						
3 mA	I_{OL}	V_{OL} = 0.4V	3			mA
6 mA	I_{OL}	V_{OL} = 0.4V	6			mA
9 mA	I_{OL}	V_{OL} = 0.4V	9			mA
12 mA	I_{OL}	V_{OL} = 0.4V	12			mA
18 mA	I_{OL}	V_{OL} = 0.4V	18			mA
24 mA	I_{OL}	V_{OL} = 0.4V	24			mA
5V-tolerant buffers						
1 mA	I_{OL}	V_{OL} = 0.4V	1			mA
2 mA	I_{OL}	V_{OL} = 0.4V	2			mA
3 mA	I_{OL}	V_{OL} = 0.4V	3			mA
6 mA	I_{OL}	V_{OL} = 0.4V	6			mA
9 mA	I_{OL}	V_{OL} = 0.4V	9			mA
12 mA	I_{OL}	V_{OL} = 0.4V	12			mA
Low-level output voltage						
3V buffers	V_{OL}	I_{OL} = 0 mA			0.1	V
5V-tolerant buffers	V_{OL}	I_{OL} = 0 mA			0.1	V
High-level output voltage						
3V buffers	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.1			V
5V-tolerant buffers	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.2			V

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  Tigard, OR 97223

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  FAX 503-643-5911

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- 16475 Dallas Parkway, Suite 380
  Dallas, TX 75248

  TEL 972-735-7444
  FAX 972-931-8680

- Research Triangle Park
  2000 Regency Parkway, Suite 455
  Cary, NC 27511

  TEL 919-460-1890
  FAX 919-469-5926

- Two Chasewood Park
  20405 SH 249, Suite 580
  Houston, TX 77070

  TEL 713-320-0524
  FAX 713-320-0574

NORTH CENTRAL/NORTHEAST

- The Meadows, 2nd Floor
  161 Worcester Road
  Framingham, MA 01701

  TEL 508-935-2200
  FAX 508-935-2234

- Greenspoint Tower
  2800 W. Higgins Road, Suite 765
  Hoffman Estates, IL 60195

  TEL 708-519-3945
  FAX 708-882-7564

THIRD-PARTY DESIGN CENTERS

SOUTH CENTRAL/SOUTHEAST

- Koos Technical Services, Inc.
  385 Commerce Way, Suite 101
  Longwood, FL 32750

  TEL 407-260-8727
  FAX 407-260-6227

- Integrated Silicon Systems Inc.
  2222 Chapel Hill Nelson Highway
  Durham, NC 27713

  TEL 919-361-5814
  FAX 919-361-2019

- Applied Systems, Inc.
  1761 W. Hillsboro Blvd., Suite 328
  Deerfield Beach, FL 33442

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