2Mx64 3.3V Simultaneous Operation Multi-Chip Package *Preliminary

FEATURES

- Access Times of 100, 120, 150ns
- Packaging
  - 119 ball stacked TSOP BGA
- 1,000,000 Erase/Program Cycles
- Sector Architecture
  - One 16KByte, two 8KBytes, one 32KByte, and fifteen 64kBytes in byte mode
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 2Mx64
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Simultaneous Read/Write Operation
  - Data can be continuously read from one bank while executing erase/program functions in other banks
- Embedded Erase and Program Algorithms
- $\overline{\text{Erase}}$ Suspend/Resume
  - Supports reading data from or programing data to a sector not being erased
- Data Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
  - Reduces overall programming time when issuing multiple program command sequences
- Ready/$\overline{\text{Busy}}$ output (RY/$\overline{\text{BY}}$)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method of resetting the internal state machine to the read mode
- $\overline{\text{WP}}$/ACC input pin
  - Write protect (WP#) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector Protection
  - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

Note: This data sheet describes a product that is not fully qualified or characterized and is subject to change without notice.

Note: For programming information refer to Flash Programming WEDPF2M64-XXX3 Application Note.

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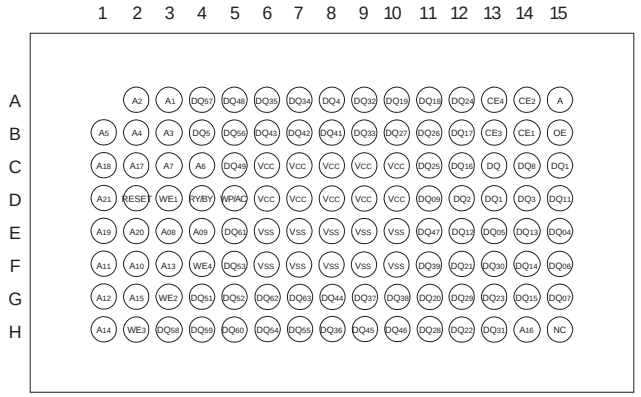
PIN CONFIGURATION FOR WF1M32B-XG2TX3

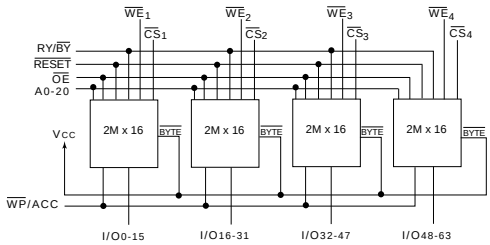
TOP VIEW



PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-19}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RESET}$	Reset/Powerdown
V_{CC}	Power Supply
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to V_{CC} +0.5	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CS_{1-4} capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	0.7 x V_{CC}	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 3.6, V_{IN} = GND or V_{CC}				10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 3.6, V_{IN} = GND or V_{CC}				10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz				65	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}				120	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 3.6, CS = V_{IH}, f = 5MHz				20	mA
V_{CC} Reset Current (2)	I_{CC4}	$\overline{RESET}$ = V_{SS} ± 0.3V			1	20	mA
Automatic Sleep Mode (2,4)	I_{CC5}	V_{IH} = V_{CC} ± 0.3 V; V_{IL} = V_{SS} ± 0.3 V			1	20	mA
V_{CC} Active Read-While-Program Current (1,2)	I_{CC6}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Word		86	180	mA
V_{CC} Active Program-While-Erase Current (1,2)	I_{CC7}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Word		85	180	mA
V_{CC} Active Program-While-Erase-Suspended Current (2,5)	I_{CC8}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	A_{CC} Pin		70	140	mA
A_{CC} Accelerated Program Current	I_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			60	120	mA
Output Low Voltage	V_{OL}	I_{OL} = 5.8 mA, V_{CC} = 3.0				0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{CC} = 3.0		0.85 x V_{CC}			V
Low V_{CC} Lock-Out Voltage (4)	V_{LKO}			2.3		2.5	V

NOTES:
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V
4. Guaranteed by design, but not tested.

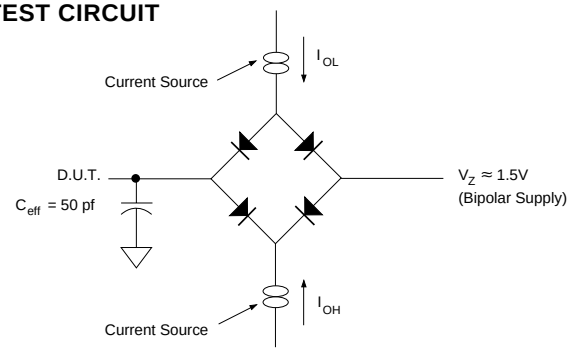
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time	t_{WHWH2}			15		15		15	sec
Read Recovery Time (2)	t_{GHEL}		0		0		0		µs
Chip Programming Time				50		50		50	sec

1. Typical value for t_{WHWH1} is 9µs.
2. Guaranteed by design, but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		65		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	50		50		65		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	50		50		65		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase	t_{WHWH2}			15		15		15	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		0		µs
V_{CC} Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time				50		50		50	sec
Output Enable Setup Time		t_{OES}	0		0		0		ns
Output Enable Hold Time (2)		t_{OEH}	10		10		10		ns
Address Setup Time to OE# low during toggle bit polling		t_{ASO}	7				15		ns
Address Hold Time From CE# or OE# high during toggle		t_{AHT}	0		0		0		ns
Output Enable High during toggle bit polling		t_{OEPH}	20		20		20		ns
Latency Between Read and Write Operations		$t_{TS/W}$	0		0		0		ns
Accelerated Programming Operation		t_{WHWH1}	4		4		4		µs
Write Recovery Time from RY/BY#		t_{RB}	0		0		0		ns
Program/Erase Valis to RY.BY#		t_{BUSY}	90		90		90		ns

1. Typical value for tWHWH1 is 9µs.
2. For Toggle and Data Polling.
3. Guaranteed by design, but not tested.

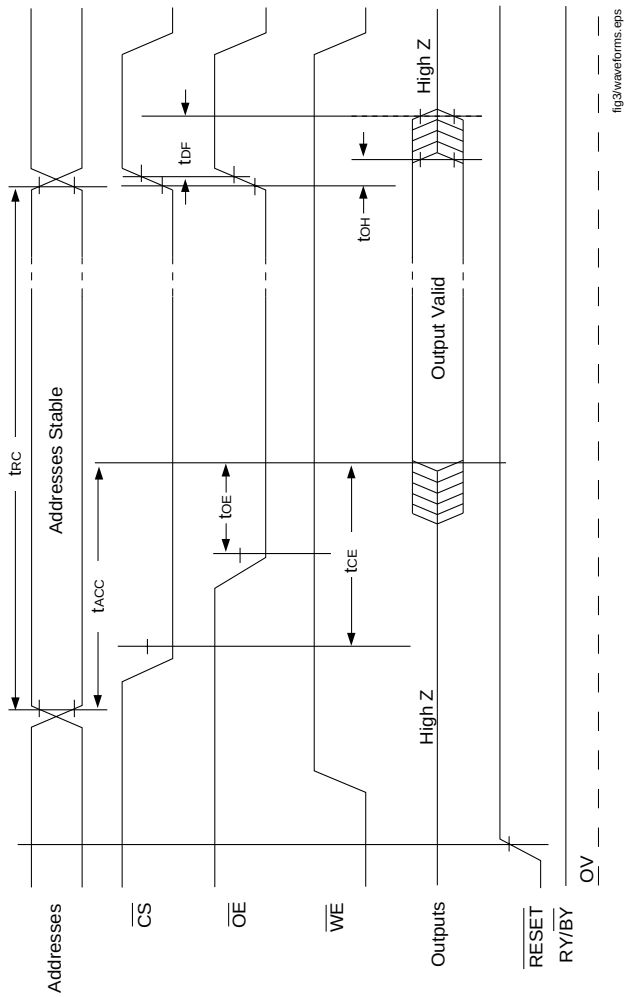
AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 3.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)	t_{EHQZ}	t_{DF}		30		30		40	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		30		30		40	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		0		0		ns

1. Guaranteed by design, not tested.

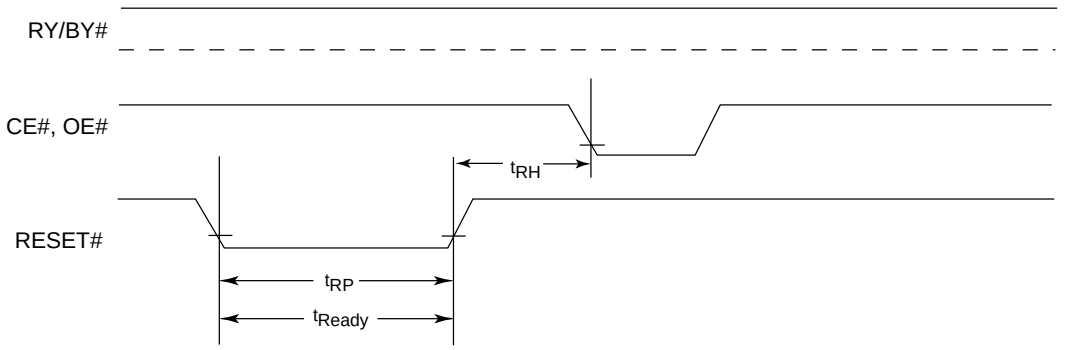
AC WAVEFORMS FOR READ OPERATIONS



AC CHARACTERISTICS – HARDWARE RESET (RESET#)

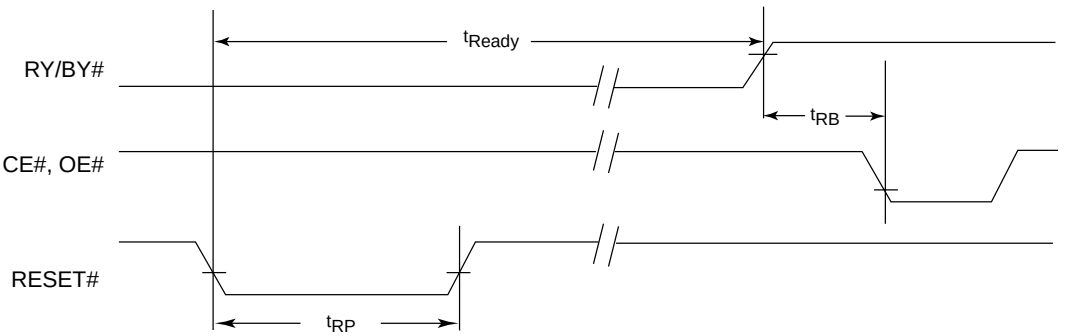
Parameter	Symbol		-100 Min	-100 Max	-120 Min	-120 Max	-150 Min	-150 Max	Unit
RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	t_{ready}			20		20		20	µs
RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	t_{ready}			500		500		500	ns
RESET # Pulse Width	t_{RP}		500		500		500		ns
RESET High Time Before Read (See Note)	t_{RH}		50		50		50		ns
RESET # Low to Standby Mode	t_{RPD}		20		20		20		µs
RY/BY# Recovery Time	t_{RB}		0		0		0		ns

Note: Not 100% tested.

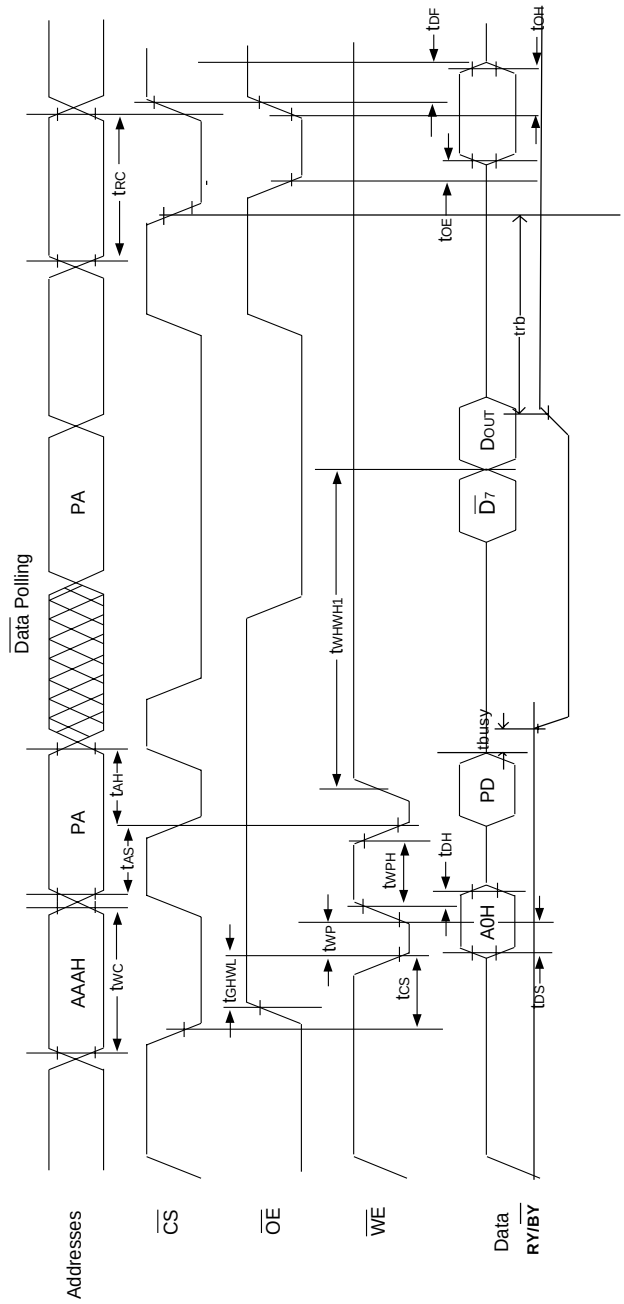


Reset Timings NOT during Embedded Algorithms

Reset Timings during Embedded Algorithms



WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED

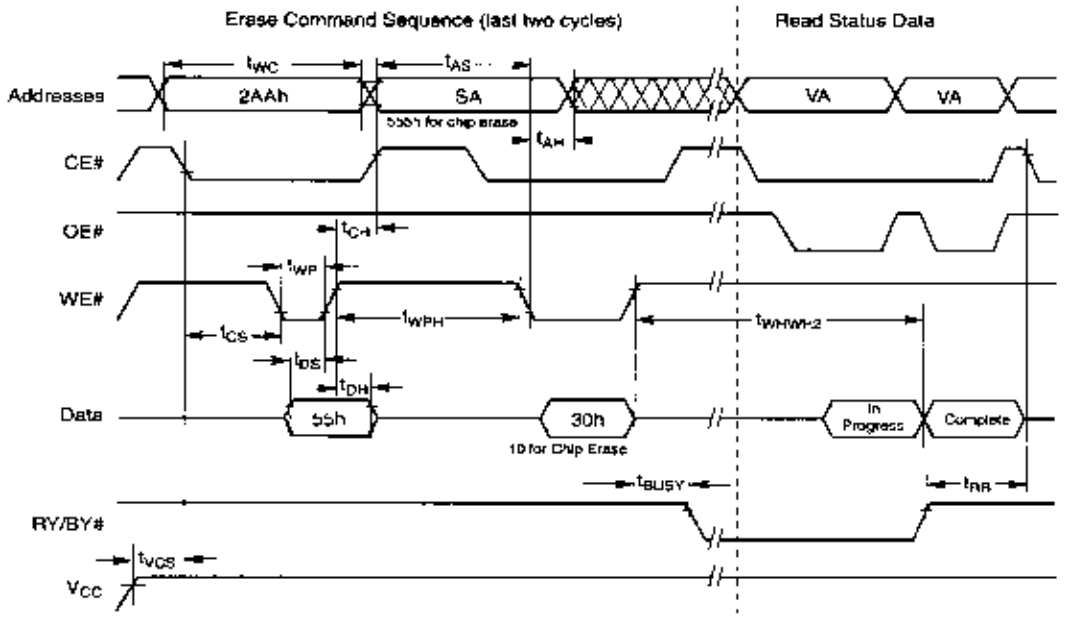


NOTES:
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

PRELIMINARY

AC CHARACTERISTICS



Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

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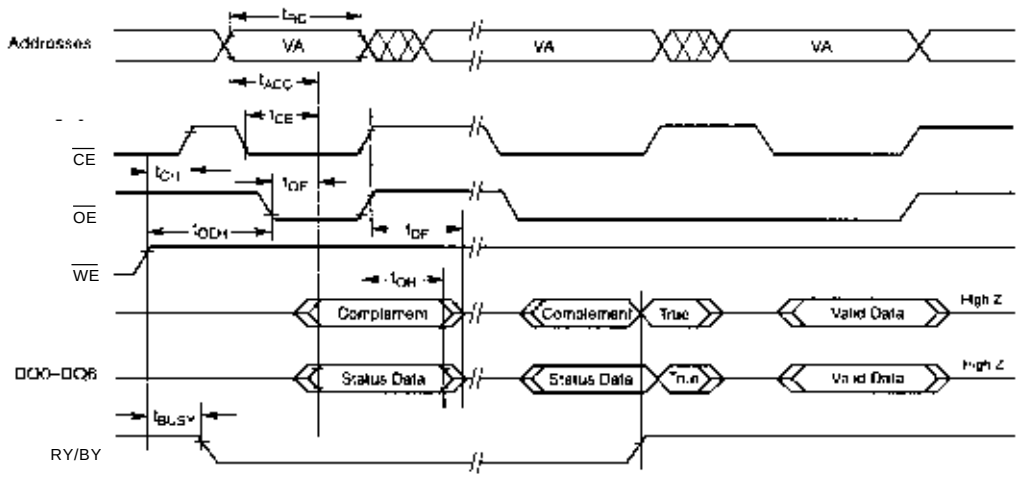
Figure 19. Chip/Sector Erase Operation Timings

NOTE:
1. SA is the sector address for Sector Erase.

AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

Figure 20. Back-to-back Read/Write Cycle Timings



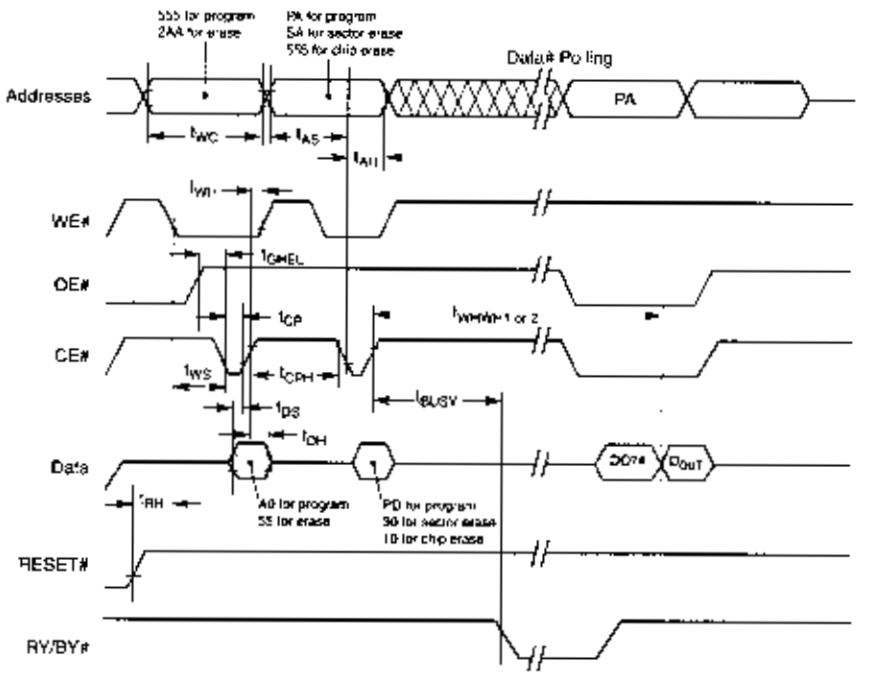
Note: VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

Fig. 21 $\overline{\text{Data}}$ Polling Timings (During Embedded Algorithms)

ALTERNATE $\overline{CS}$ CONTROLLED PROGRAMMING OPERATION TIMINGS

PRELIMINARY

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

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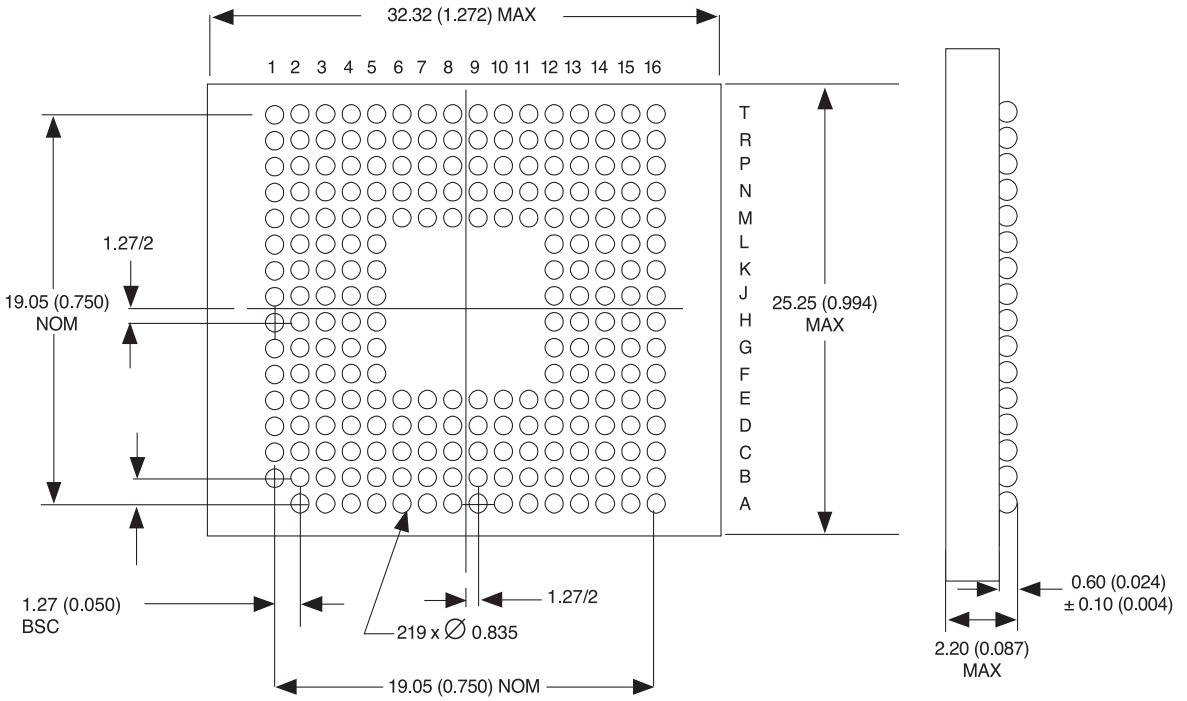
Figure 26. Alternate CE# Controlled Write (Erase/Program) Operation Timings

NOTES:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

PACKAGE 509: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 401: **66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION