



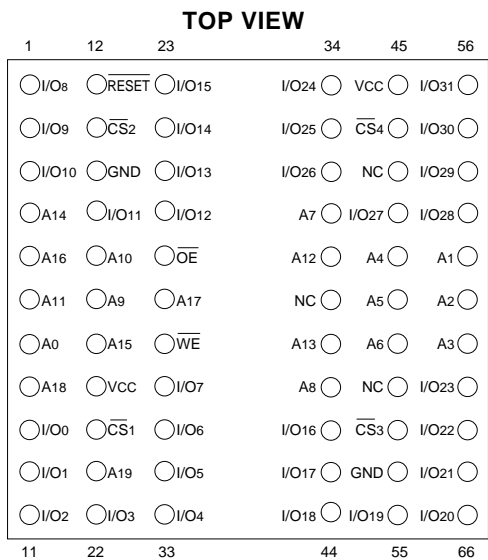
1Mx32 5V FLASH MODULE *ADVANCED**

FEATURES

- Access Times of 70, 90, 120ns
- Packaging:
 - 66 pin, PGA Type, 1.185" square, Hermetic Ceramic HIP (Package 401)
 - 68 lead, 22mm Low Profile CQFP, 4.6mm (0.180"), (Package 509)
- Sector Architecture
 - One 16KByte Sectors
 - Two 8KByte Sectors
 - One 32KByte Sectors
 - Fifteen 64KByte Sectors
- 1,000,000 Erase/Program Cycles
- Organized as 1Mx32, user configurable as 2Mx16 or 4Mx8.
- Commercial, Industrial and Military Temperature Ranges
- 5V ± 10% for Read and Write Operations.
- Low Power CMOS
- Embedded Erase and Program Algorithm
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
WEDF1M32B-XG2TX5 - 8 grams typical
WEDF1M32B-XHX5 - 13 grams typical

** This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WEDF1M32B-XHX5



PIN DESCRIPTION

| | |
|---------|---------------------|
| I/O0-31 | Data Inputs/Outputs |
| A0-19 | Address Inputs |
| WE | Write Enable |
| CS1-4 | Chip Selects |
| OE | Output Enable |
| RESET | Reset |
| Vcc | Power Supply |
| GND | Ground |
| NC | Not Connected |

BLOCK DIAGRAM

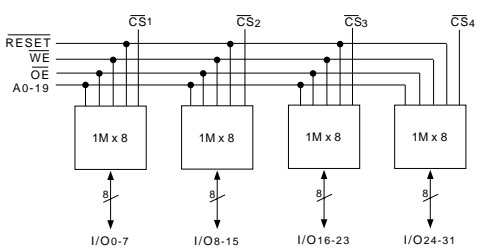
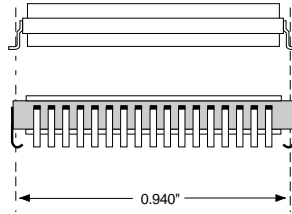
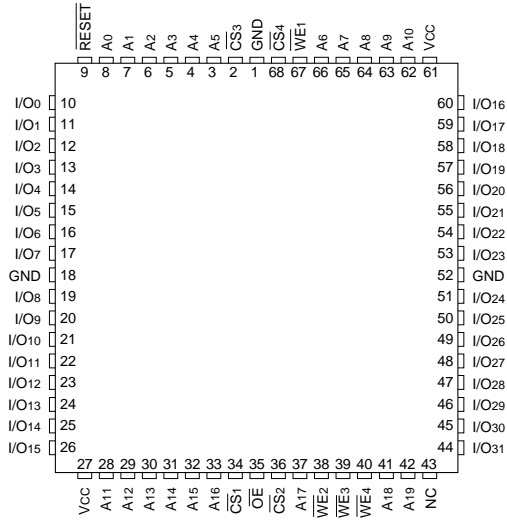




FIG. 2 PIN CONFIGURATION FOR WEDF1M32B-XG2TX5

TOP VIEW

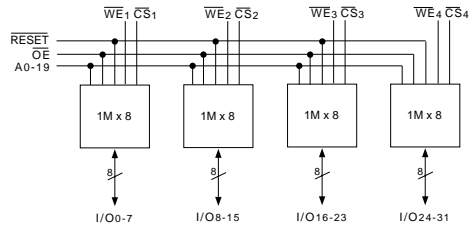


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

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| NC | Not Connected |

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

| Parameter | | Unit |
|--|---------------|------|
| Voltage on Any Pin with Respect to GND – V _{CC} and V _{PP}) | -0.5 to +7.0 | V |
| Voltage with Respect to GND – A ₉ , \overline{OE} , and RESET (2) | -2.0 to +12.5 | V |
| Voltage with Respect to GND – All other pins (1) | -2.0 to +7.0 | V |
| Output Short Circuit Current | 200 | mA |

NOTES:

1. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V which, during transitions, may overshoot to V_{CC} + 2.0V for periods <20ns.
2. Minimum DC input voltage on pins A₉, \overline{OE} , and RESET is -0.5V. During voltage transitions, A₉, \overline{OE} , and RESET may undershoot V_{SS} to -2.0V for periods of up to 20ns. See Figure 6. Maximum DC input voltage on pin A₉ is +12.5V which may overshoot to +13.5V for periods up to 20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a Stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|------------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 4.5 | 5.5 | V |
| Input High Voltage | V _{IH} | 2.0 | V _{CC} + 0.5 | V |
| Input Low Voltage | V _{IL} | -0.5 | +0.8 | V |
| Operating Temp. (Mil.) | T _A | -55 | +125 | °C |

CAPACITANCE

(T_A = +25°C)

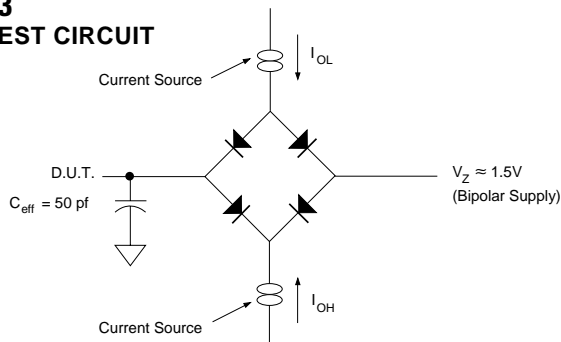
| Parameter | Symbol | Conditions | Max | Unit |
|---------------------------------|------------------|-------------------------------------|-----|------|
| \overline{OE} capacitance | C _{OE} | V _{IN} = 0 V, f = 1.0 MHz | 50 | pF |
| \overline{WE} 1-4 capacitance | C _{WE} | V _{IN} = 0 V, f = 1.0 MHz | 20 | pF |
| \overline{CS} 1-4 capacitance | C _{CS} | V _{IN} = 0 V, f = 1.0 MHz | 20 | pF |
| Data I/O capacitance | C _{I/O} | V _{I/O} = 0 V, f = 1.0 MHz | 20 | pF |
| Address input capacitance | C _{AD} | V _{IN} = 0 V, f = 1.0 MHz | 50 | pF |

This parameter is guaranteed by design but not tested.

DATA RETENTION

| Parameter | Test Conditions | Min | Unit |
|----------------------|-----------------|-----|-------|
| Minimum Pattern Data | 150°C | 10 | Years |
| Retention Time | 125°C | 20 | Years |

**FIG. 3
AC TEST CIRCUIT**



AC TEST CONDITIONS

| Parameter | Typ | Unit |
|----------------------------------|--|------|
| Input Pulse Levels | V _{IL} = 0, V _{IH} = 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

NOTES:

- V_Z is programmable from -2V to +7V.
- I_{OL} & I_{OH} programmable from 0 to 16mA.
- Tester Impedance Z₀ = 75 Ω.
- V_Z is typically the midpoint of V_{OH} and V_{OL}.
- I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.



DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|------------------|---|-----|------|------|
| Input Leakage Current | I _{LI} | V _{IN} = V _{CC} to GND | | 10 | μA |
| Output Leakage Current | I _{LO} | V _{OUT} = V _{CC} to GND | | 10 | μA |
| V _{CC} Read Current (1,2) | I _{CC1} | $\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5 \text{ MHz}, I_{OUT} = 0 \text{ mA}$ | | 160 | mA |
| V _{CC} Write Current (2,3,4) | I _{CC2} | $\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$ | | 200 | mA |
| V _{CC} Standby Current (2,5) | I _{CC3} | $\overline{CS} = \overline{RESET} = \overline{OE} = V_{IH}, f = 5 \text{ MHz}$ | | 20.0 | mA |
| Output Low Voltage | V _{OL} | V _{CC} = 4.5, I _{OL} = 5.8 mA | | 0.45 | V |
| Output High Voltage | V _{OH} | V _{CC} = 4.5, I _{OH} = -2.5 mA | 2.4 | | V |
| Low V _{CC} Lockout Voltage (4) | V _{LKO} | | 3.2 | 4.2 | V |

NOTES:

- The I_{CC} current listed is typically less than 2mA/MHz, with \overline{OE} at V_{IH}.
- Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} max.
- I_{CC} active while Embedded Erase or Embedded Program is in progress.
- Not 100% tested.
- I_{CC3} = 20μA max at extended temperature (> +85°C).

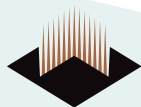
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - \overline{WE} CONTROLLED

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

| Parameter | Symbol | | -70 | | -90 | | -120 | | Unit |
|-------------------------------|--------------------|------------------|-----|-----|-----|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | t _{AVAV} | t _{WC} | 70 | | 90 | | 120 | | ns |
| Chip Select Setup Time | t _{ELWL} | t _{CS} | 0 | | 0 | | 0 | | ns |
| Write Enable Pulse Width | t _{WLWH} | t _{WP} | 35 | | 45 | | 50 | | ns |
| Address Setup Time | t _{AVWH} | t _{AS} | 0 | | 0 | | 0 | | ns |
| Data Setup Time | t _{DVWH} | t _{DS} | 30 | | 45 | | 50 | | ns |
| Data Hold Time | t _{WHDX} | t _{DH} | 0 | | 0 | | 0 | | ns |
| Address Hold Time | t _{WHAX} | t _{AH} | 45 | | 45 | | 50 | | ns |
| Chip Select Hold Time | t _{WHEH} | t _{CH} | 0 | | 0 | | 0 | | ns |
| Write Enable Pulse Width High | t _{WHWL} | t _{WPH} | 20 | | 20 | | 20 | | ns |
| Programming Operation (2) | t _{WHWH1} | | | 300 | | 300 | | 300 | μs |
| Sector Erase Operation (3) | t _{WHWH2} | | | 8 | | 8 | | 8 | sec |
| Write Recovery before Read | t _{WHGL} | | 0 | | 0 | | 0 | | μs |
| Chip Programming Time | | | | 50 | | 50 | | 50 | sec |

NOTES:

- Guaranteed by design, not tested.
- Typical value for t_{WHWH1} is 7μs.
- Typical value for t_{WHWH2} is 1sec.



AC CHARACTERISTICS – WRITE OPERATION - \overline{CS} CONTROLLED ⁽¹⁾

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

| Parameter | Symbol | | -70 | | -90 | | -120 | | Unit |
|------------------------------|--------------------|------------------|-----|-----|-----|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Write Enable Cycle Time | t _{AVAV} | t _{WC} | 70 | | 90 | | 120 | | ns |
| Write Enable Setup Time | t _{WLEL} | t _{WS} | 0 | | 0 | | 0 | | ns |
| Chip Select Pulse Width | t _{TELEH} | t _{CP} | 35 | | 45 | | 50 | | ns |
| Address Setup Time | t _{AVEH} | t _{AS} | 0 | | 0 | | 0 | | ns |
| Data Setup Time | t _{DVEH} | t _{DS} | 30 | | 45 | | 50 | | ns |
| Data Hold Time | t _{EHDX} | t _{DH} | 0 | | 0 | | 5 | | ns |
| Address Hold Time | t _{EHAX} | t _{AH} | 45 | | 45 | | 50 | | ns |
| Write Enable Hold Time | t _{EHWH} | t _{WH} | 0 | | 0 | | 0 | | ns |
| Chip Select Pulse Width High | t _{EHEL} | t _{EPH} | 20 | | 20 | | 20 | | ns |
| Programming Operation (1) | t _{WHWH1} | | | 300 | | 300 | | 300 | μs |
| Sector Erase Operation (2) | t _{WHWH2} | | | 8 | | 8 | | 8 | sec |
| Write Recovery before Read | t _{EHGL} | | 0 | | 0 | | 0 | | μs |

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.

AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

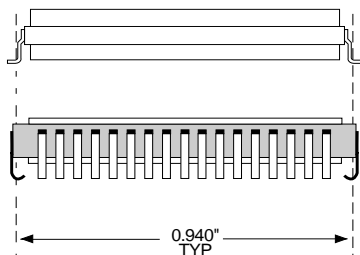
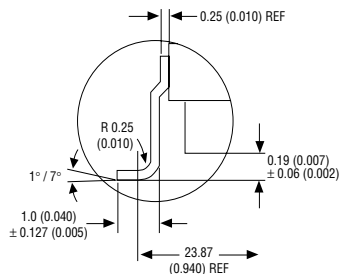
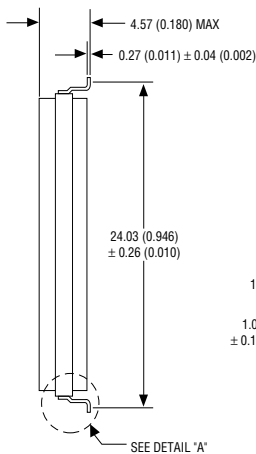
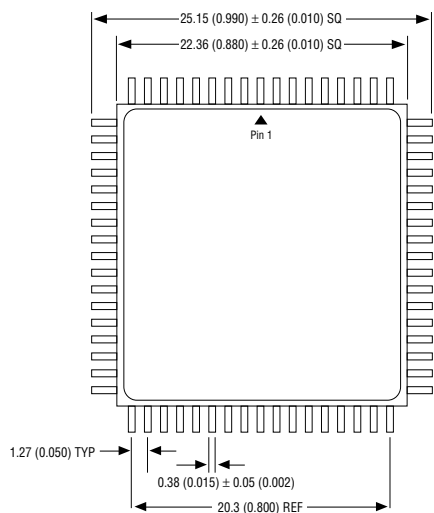
| Parameter | Symbol | | -70 | | -90 | | -120 | | Unit |
|---|-------------------|------------------|-----|-----|-----|-----|------|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | t _{AVAV} | t _{RC} | 70 | | 90 | | 120 | | ns |
| Address Access Time | t _{AVQV} | t _{ACC} | | 70 | | 90 | | 120 | ns |
| Chip Select to Output Valid (1) | t _{ELQV} | t _{CE} | | 70 | | 90 | | 120 | ns |
| Output Enable to Output Valid (1) | t _{GLQV} | t _{OE} | | 30 | | 35 | | 50 | ns |
| Chip Select to Output Low Z (2) | t _{ELQX} | t _{LZ} | 0 | | 0 | | 0 | | ns |
| Chip Select High to Output High Z (2) | t _{EHQZ} | t _{HZ} | | 20 | | 20 | | 50 | ns |
| Output Enable to Output Low Z (2) | t _{GLQX} | t _{OLZ} | 0 | | 0 | | 0 | | ns |
| Output Enable High to Output High Z (2) | t _{GHQZ} | t _{DF} | | 20 | | 20 | | 30 | ns |
| Output Hold from Addresses, \overline{CS} or \overline{OE} Change, Whichever is First (2) | | t _{OH} | 0 | | 0 | | 0 | | ns |

NOTES:

1. \overline{OE} may be delayed up to t_{CE-t_{OE}} after the falling edge of \overline{CS} without impact on t_{CS}.
2. Guaranteed by design, not tested.



PACKAGE 509: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2T)

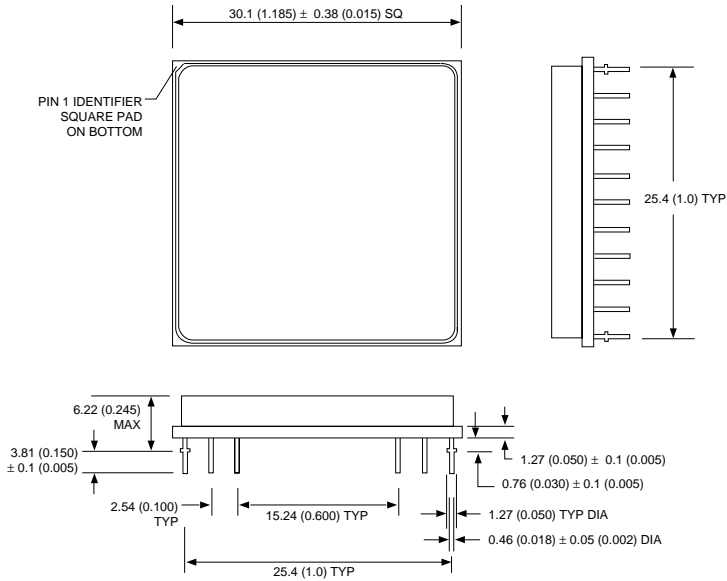


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ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



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ORDERING INFORMATION

WED F 1M32 B - XXX X X 5 X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE

5 = 5V

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H = Ceramic Hex-In-Line Package, HIP (Package 401)

G2T = 22mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 509)

ACCESS TIME (ns)

Bottom Boot Block

ORGANIZATION, 1M x 32

User configurable as 2M x 16 or 4M x 8

Flash

WHITE ELECTRONIC DESIGNS CORP.