



2, 4, and 8MB, STmicro, 5.0V 4Mb Based, Uniform Sector FLASH Module Family

FEATURES

- 2, 4, and 8MB Density FLASH Modules
- Organized as; 512K x 32, 2 x 512K x 32, and 4 x 512K x 32
- Based on STmicro's M29F040B 5.0V FLASH Device
- Base Component DEVICE ID = E2h
- Base Component MANUFACTURERS ID = 20h
- Uniform Sector Architecture
- Sector Erase
- Sector Protection
- Embedded Erase Algorithm
- Embedded Program Algorithm (AMD Compatible)
- Data Polling and Toggle Bit for Detection
- 100,000 Program/Erase Cycles per Block
- 20 Year Data Retention

DESCRIPTION

The WED7F325ZXEBN, WED7F2325ZXEBN, and WED7F4325ZXEBN are organized as 512K x 32, 2 x 512K x 32 and 4 x 512K x 32 respectively. The modules are based on 4Mb TSOP components from STmicro which are mounted onto an FR4 substrate.

The Modules are offered in Access Speeds from 70 to 150ns with an Operation Voltage Requirement of 5.0V ±10%.

PIN CONFIGURATION

PIN#	PIN Name	PIN#	PIN Name	PIN#	PIN Name	PIN#	PIN Name
1	V _{SS}	21	(Note 1)	41	A ₁₁	61	DQ ₉
2	V _{CC}	22	(Note 1)	42	A ₁₀	62	DQ ₈
3	NC	23	(Note 1)	43	A ₉	63	DQ ₇
4	\bar{G}	24	(Note 1)	44	A ₈	64	DQ ₆
5	\bar{W}_0	25	V _{SS}	45	A ₇	65	DQ ₅
6	\bar{W}_1	26	DQ ₂₉	46	A ₆	66	DQ ₄
7	NC	27	DQ ₃₀	47	A ₅	67	DQ ₃
8	DQ ₁₆	28	DQ ₃₁	48	A ₄	68	DQ ₂
9	DQ ₁₇	29	\bar{W}_2	49	A ₃	69	DQ ₁
10	DQ ₁₈	30	NC	50	A ₂	70	DQ ₀
11	DQ ₁₉	31	NC	51	A ₁	71	NC
12	DQ ₂₀	32	NC	52	A ₀	72	V _{CC}
13	DQ ₂₁	33	NC	53	\bar{W}_3	73	PD ₁
14	DQ ₂₂	34	A ₁₈	54	V _{SS}	74	PD ₂
15	DQ ₂₃	35	A ₁₇	55	DQ ₁₅	75	PD ₃
16	DQ ₂₄	36	A ₁₆	56	DQ ₁₄	76	PD ₄
17	DQ ₂₅	37	A ₁₅	57	DQ ₁₃	77	PD ₅
18	DQ ₂₆	38	A ₁₄	58	DQ ₁₂	78	PD ₆
19	DQ ₂₇	39	A ₁₃	59	DQ ₁₁	79	PD ₇
20	DQ ₂₈	40	A ₁₂	60	DQ ₁₀	80	V _{SS}

Note 1: Bank Enable

SIMM Density	Pin 24	Pin 23	Pin 22	Pin 21
512K x 32	E ₀	NC	NC	NC
2 x 512K x 32	E ₀	E ₁	NC	NC
4 x 512K x 32	E ₀	E ₁	E ₂	E ₃

PRESENCE DETECT PINS; MODULE DENSITY

SIMM Density	Presence Select Pin			
	PD ₁	PD ₂	PD ₃	PD ₄
512K x 32	V _{SS}	V _{SS}	V _{SS}	Open
2 x 512K x 32	Open	Open	Open	V _{SS}
4 x 512K x 32	V _{SS}	Open	Open	V _{SS}

PIN CAPACITANCE

Parameter	Sym	Pins	2MB Value	4MB Value	8MB Value
Input Capacitance	C _{in}	Address	20pF	40pF	80pF
Input Capacitance	C _{in}	\bar{G}	20pF	40pF	80pF
Output Capacitance	C _{io}	Input/Output Data Bus	5pF	10pF	20pF
Input Capacitance	C _{in}	\bar{E}_{0-3}	20pF	20pF	20pF
Input Capacitance	C _{in}	\bar{W}_{0-3}	5pF	10pF	20pF

PIN NAME, DEFINITION

A ₀₋₁₉	Address Inputs
DQ ₀₋₃₁	Common Data Input/ Output
\bar{W}_{0-3}	Byte Write Enables
\bar{E}_{0-3}	Bank Enable
\bar{G}	Output Enable
PD ₀₋₇	Presence Detect
NC	No Connect
V _{CC}	Power 5V ±10%
V _{SS}	Ground



ORDERING INFORMATION

2MB, 512K X 32

Part Number	Density	Speed	Package
WED7F325ZXEBN70C	2MB	70ns	366
WED7F325ZXEBN90C	2MB	90ns	366
WED7F325ZXEBN12C	2MB	120ns	366
WED7F325ZXEBN15C	2MB	150ns	366

8MB, 4 X 512K X 32

Part Number	Density	Speed	Package
WED7F4325ZXEBN90C	8MB	90ns	368
WED7F4325ZXEBN12C	8MB	120ns	368
WED7F4325ZXEBN15C	8MB	150ns	368

4MB, 2 X 512K X 32

Part Number	Density	Speed	Package
WED7F2325ZXEBN70C	4MB	70ns	367
WED7F2325ZXEBN90C	4MB	90ns	367
WED7F2325ZXEBN12C	4MB	120ns	367
WED7F2325ZXEBN15C	4MB	150ns	367

FIG. 1

**FUNCTIONAL BLOCK DIAGRAM
2MB; 512K X 32**

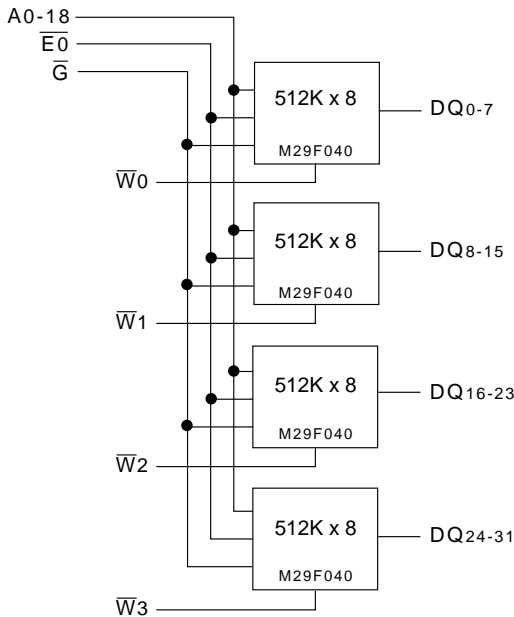


FIG. 2

**FUNCTIONAL BLOCK DIAGRAM
4MB; 2 X 512K X 32**

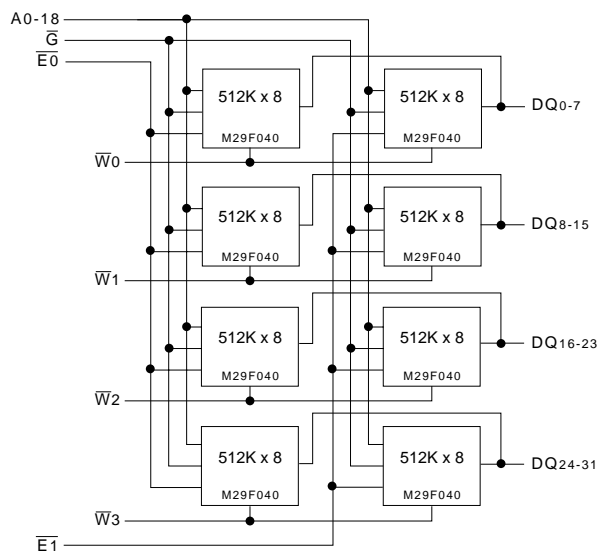




FIG. 3

FUNCTIONAL BLOCK DIAGRAM
8MB; 4 X 512K X 32

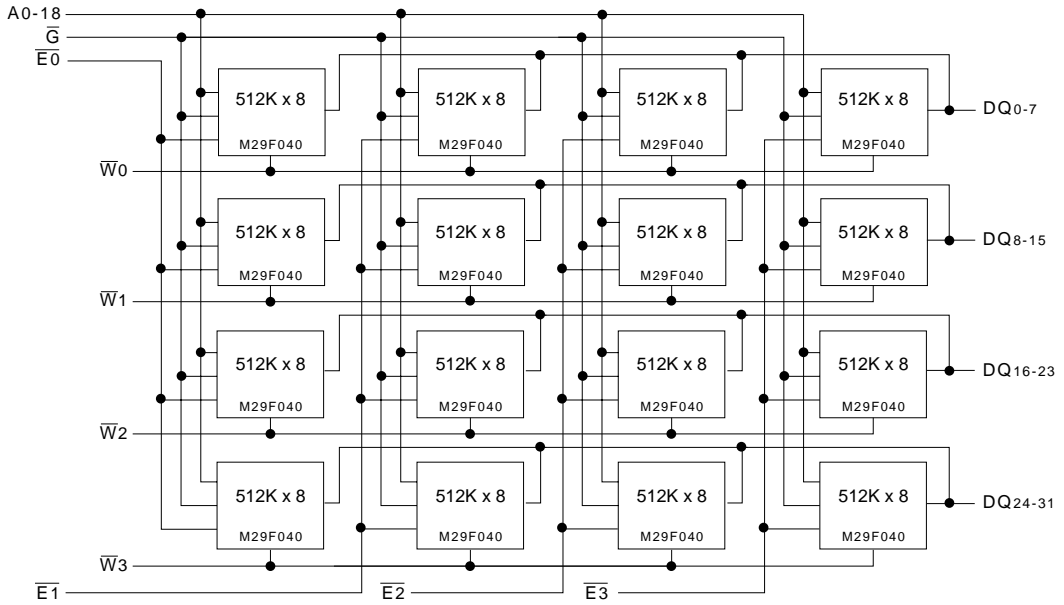


FIG. 4

MECHANICAL; PACKAGE - 366

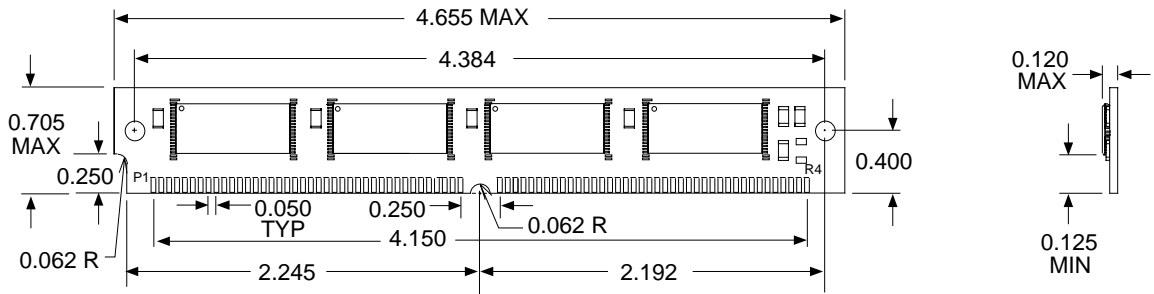




FIG. 5
MECHANICAL; PACKAGE - 367

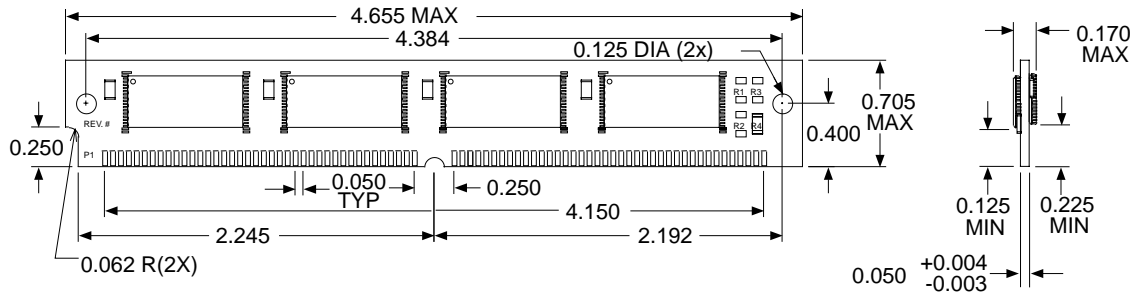


FIG. 6
MECHANICAL; PACKAGE - 368

