

256Kx1 High Speed Monolithic SRAM CMOS

FEATURES

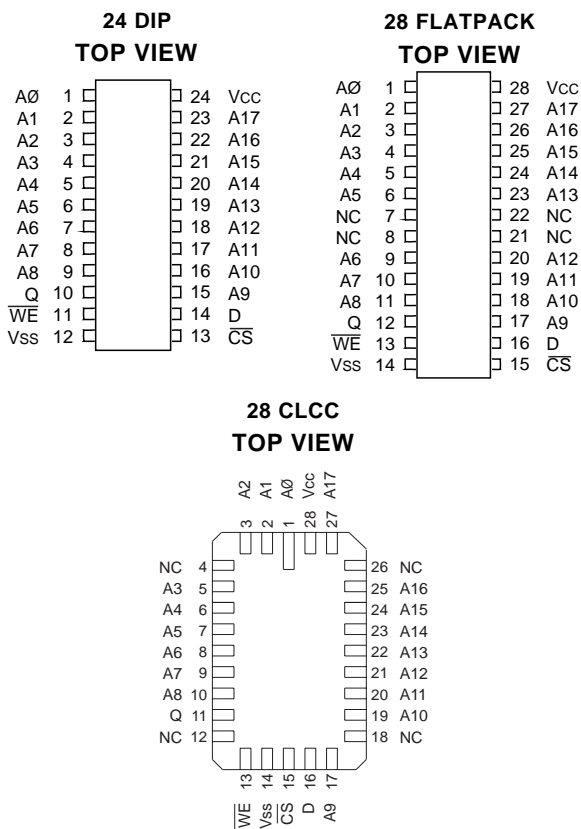
- 128Kx8 bit CMOS Static
- Random Access Memory
 - Fast Access Times of 35, 45, 55ns
 - Data Retention Function (LP)
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- JEDEC Approved Pinouts
 - 24 pin Ceramic DIP (Package 3)
 - 28 pad Ceramic LCC (Package 14)
 - 28 lead Ceramic Flatpack (Package 79)
- Single +5V (±10%) Supply Operation

The EDI88128CS is a high speed, high performance, megabit density Monolithic CMOS Static RAM organized as 128Kx8.

The device has eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

A Low Power version with 2V Data Retention (EDI88128LPS) is also available for battery back-up operation. Military product is available compliant of MIL-PRF-38535.

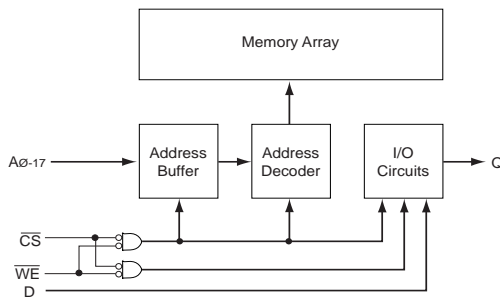
FIG. 1 PIN CONFIGURATION



PIN DESCRIPTION

D	Data Input
Q	Data Output
A0-17	Address Inputs
WE	Write Enable
CS	Chip Select
Vcc	Power (+5V ±10%)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature TA (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, TJ	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	Output	Power
H	X	Standby	High Z	Icc2, Icc3
L	H	Output Deselect	High Z	Icc1
L	H	Read	Data Out	Icc1
L	L	Write	Data In	Icc1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	6.0	V
Input Low Voltage	V _{IL}	-0.3	—	+0.8	V

CAPACITANCE

(TA = +25°C)

Parameter	Symbol	Condition	Max	Unit
			LCC, DIP, Flatpack	
Address Lines	C _I	V _{IN} = Vcc or Vss, f = 1.0MHz	10	pF
Data Lines	C _{D/O}	V _{OUT} = Vcc or Vss, f = 1.0MHz	12	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(Vcc = 5V, TA = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = 0V to Vcc	-5	—	+5	μA
Output Leakage Current	I _{LO}	V _{I/O} = 0V to Vcc	-5	—	+5	μA
Operating Power Supply Current	Icc1	\overline{WE} , \overline{CS} = V _{IL} , I _{I/O} = 0mA, Min Cycle	—	80	120	mA
Standby (TTL) Power Supply Current	Icc2	\overline{CS} ≥ V _{IH} , V _{IN} ≤ V _{IL} , V _{IN} ≥ V _{IH}	—	2	20	mA
Full Standby Power Supply Current	Icc3	\overline{CS} ≥ Vcc - 0.2V	—	1	3	mA
		V _{IN} ≥ Vcc - 0.2V or V _{IN} ≤ 0.2V	—	0.5	1.5	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc - 0.3V



AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	35		45		55		ns
Address Access Time	t _{AVOV}	t _{AA}		35		45		55	ns
Chip Enable Access Time	t _{ELOV}	t _{ACS}		35		45		55	ns
Chip Enable to Output in Low Z (1)	t _{ELOX}	t _{CLZ}	5		5		5		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}	0	20	0	20	0	20	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	5		5		5		ns
Chip Enable to Power Up (1)	t _{ELICCH}	t _{PU}	0		0		0		ns
Chip Enable to Power Down (1)	t _{EHICCL}	t _{PD}		35		45		55	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	35		45		55		ns
Chip Enable to End of Write	t _{ELWH}	t _{CW}	30		35		45		ns
	t _{ELEH}	t _{CW}	30		35		45		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	30		35		45		ns
	t _{AVEH}	t _{AW}	30		35		45		ns
Write Pulse Width	t _{WLWH}	t _{WP}	25		25		30		ns
	t _{WLEH}	t _{WP}	25		25		30		ns
Write Recovery Time	t _{WHAX}	t _{WR}	5		5		5		ns
	t _{EHAX}	t _{WR}	5		5		5		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
	t _{EHDX}	t _{DH}	0		0		0		ns
Write to Output in High Z (1)	t _{WLOZ}	t _{WHZ}	0	15	0	15	0	20	ns
Data to Write Time	t _{DVWH}	t _{DW}	20		25		25		ns
	t _{DVEH}	t _{DW}	20		25		25		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS

Figure 1

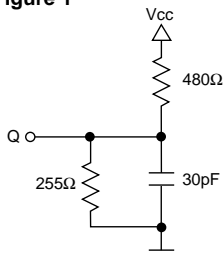
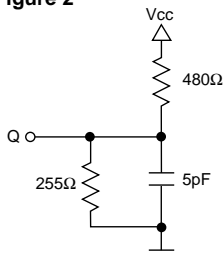


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{EHQZ} and t_{WLOZ}, C_L = 5pF (Figure 2)



FIG. 2
TIMING WAVEFORM - READ CYCLE

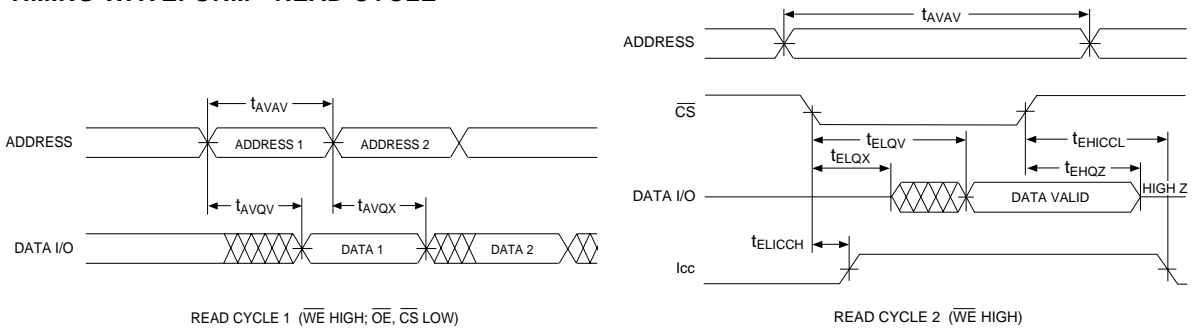


FIG. 3
WRITE CYCLE - \overline{WE} CONTROLLED

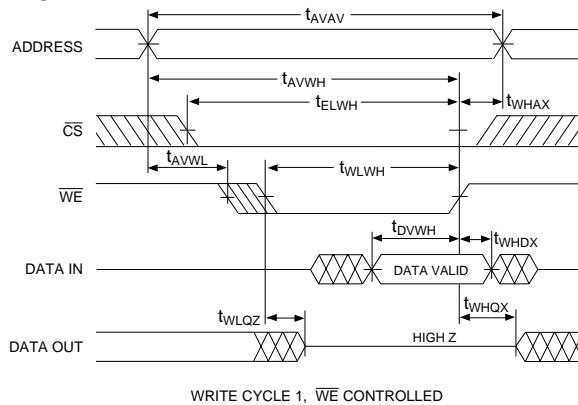
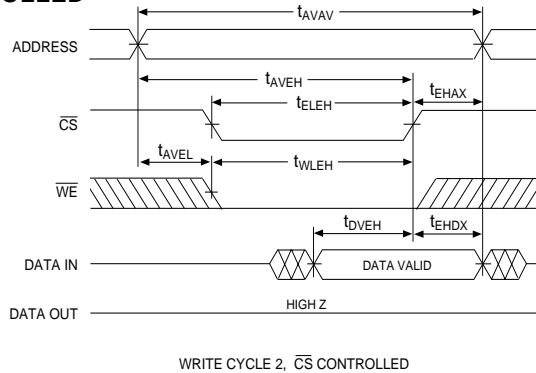


FIG. 4
WRITE CYCLE - \overline{CS} CONTROLLED





DATA RETENTION CHARACTERISTICS (EDI81256LP ONLY)

(TA = -55°C to +125°C)

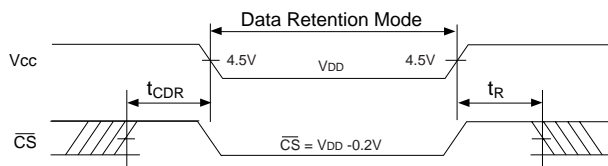
Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V _{DD}	V _{DD} = 2.0V	2	-	-	V
Data Retention Quiescent Current	I _{CCDR}	$\overline{CS} \geq V_{DD} - 0.2V$	-	50	500	μA
Chip Disable to Data Retention Time (1)	T _{CDR}	V _{IN} \geq V _{DD} - 0.2V	0	-	-	ns
Operation Recovery Time (1)	T _R	or V _{IN} \leq 0.2V	T _{AVAV} *	-	-	ns

NOTE:

1. Parameter guaranteed by design, but not tested.

* Read Cycle Time

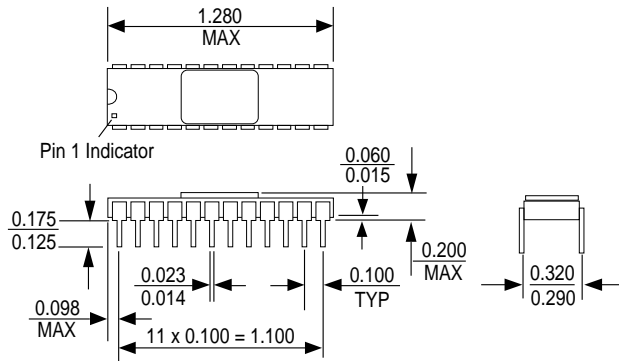
FIG. 5
DATA RETENTION - \overline{CS} CONTROLLED



DATA RETENTION, \overline{CS} CONTROLLED

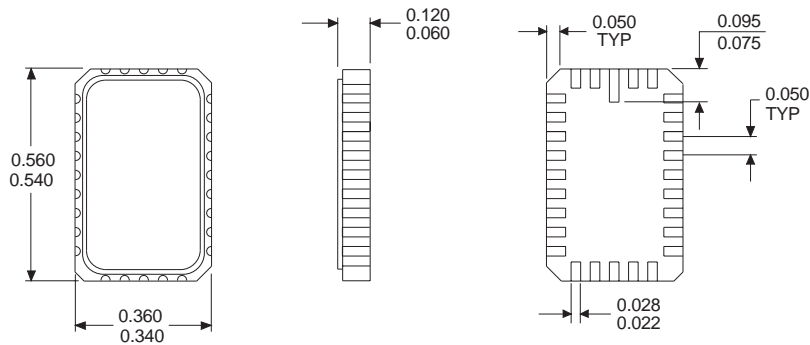


PACKAGE 3: 24 PIN SIDEBRAZED CERAMIC DIP (300 mils wide)



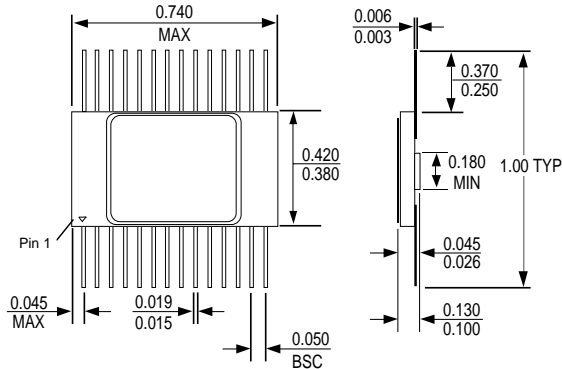
ALL DIMENSIONS ARE IN INCHES

PACKAGE 14: 28 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 79: 28 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 8 128 CS X X X

WHITE ELECTRONIC DESIGNS _____

SRAM _____

ORGANIZATION, 128Kx8 _____

TECHNOLOGY: _____

C = CMOS Standard Power

LP = Low Power

ACCESS TIME (ns) _____

PACKAGE TYPE: _____

C = 32 lead Sidebraced DIP, 300 mil (Package 3)

F = 32 lead Ceramic Flatpack (Package 79)

L = 32 pad Ceramic LCC (Package 14)

DEVICE GRADE: _____

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C