HYM532814A M-Series

8Mx32-bit CMOS SDRAM MODULE
with EXTENDED DATA OUT

DESCRIPTION

The HYM5332814A is a 8M x 32-bit EDO mode CMOS DRAM module consisting of sixteen HY5117404A in 24/26 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.1§ bnd 0.01§ bdecoupling are mounted for each DRAM. The HYM532814AM/ASLM/ATM/ASLTM are Tin-Lead plated and HYM532814AMG/ASLMG/ATMG/ASLTMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 32M byte memory.

FEATURES

- Low power dissipation
  Max. self-refresh 26.4W (SL-part)
  Max. battery back-up 52.8W (SL-part)
  Max. CMOS standby 35.2mW (SL-part)
  88.0mW
  Max. TTL standby 176.0mW
  Max. operating

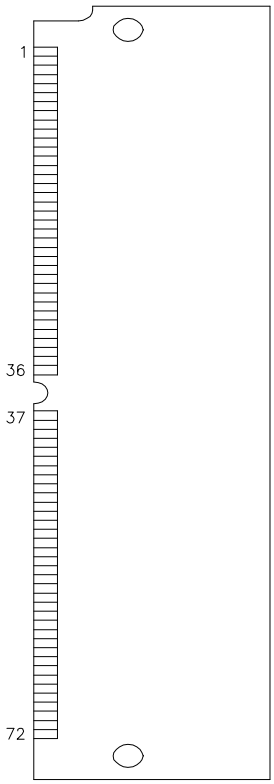
Speed	Power
60	5.37W
70	4.49W
80	4.05W

- Single power supply of 5V±10%
- TTL compatible inputs and outputs
- Fast access time

Speed	t_{RAS}	t_{CAC}	t_{HPC}
60	60ns	15ns	25ns
70	70ns	18ns	30ns
80	80ns	20ns	35ns

- EDO mode operation
- /CAS-before-/RAS, /RAS-only, Hidden refresh, Self-refresh
- 2048 refresh cycles / 256ms (SL-part)
  2048 refresh cycles / 32ms

PIN CONNECTION



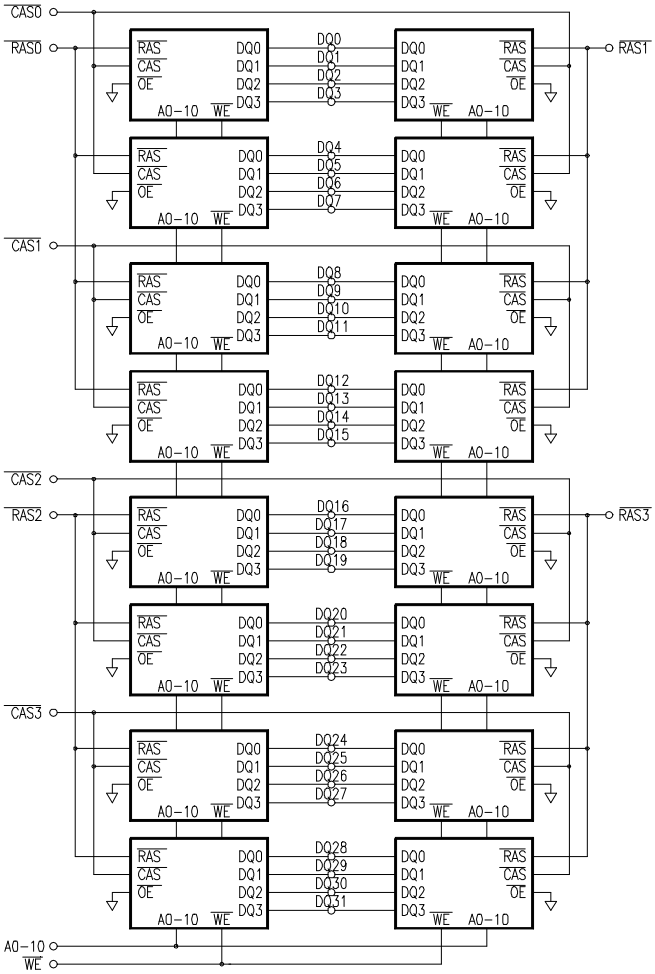
PIN CONNECTION

/RAS0-/RAS3	Row Address Strobe
/CAS0-/CAS3	Column Address Strobe
/WE	Write Enable
A0-A10	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground

PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	/CAS0
5	DQ17	41	/CAS2
6	DQ2	42	/CAS3
7	DQ18	43	/CAS1
8	DQ3	44	/RAS0
9	DQ19	45	/RAS1
10	Vcc	46	NC
11	NC	47	/WE
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	/RAS3	69	PD3
34	/RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	NC	NC	NC
PD2	Vss	Vss	Vss
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	¡ É
T_{STG}	Storage Temperature	-55 to 125	¡ É
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0¡ Éto 70¡ É

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA=0¡ Éto 70¡ ÉVCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS¡ ÎVIN¡ ÎVCC+1.0, All other pins not under test=VSS		-160	160	¥ ÌA	
ILO	Output Leakage Current (High impedance State)	VSS¡ ÎVOUT¡ Îvcc /RAS & /CAS at VIH		-20	20	¥ ÌA	
ICC1	VCC Supply Current Operating	tRC=tRC (min.)	60	-	976	mA	1,2,3
			70	-	816		
			80	-	736		
ICC2	VCC Supply Current TTL Standby	/RAS & /CAS at VIH, other inputs ≥ VSS		-	32	mA	
ICC3	VCC Supply Current /RAS-only refresh	tRC=tRC(min.)	60	-	976	mA	1,3
			70	-	816		
			80	-	736		
ICC4	VCC Supply Current, EDO mode	tHPC= tHPC (min.)	60	-	816	mA	1,2,3
			70	-	736		
			80	-	656		
ICC5	VCC Supply Current CMOS Standby	/RAS & /CAS ≥ VCC – 0.2V		-	16	mA	
			SL-part	-	6.4		5
ICC6	VCC Supply Current /CAS before /RAS refresh	tRC=tRC(min.)	60	-	976	mA	1,3
			70	-	816		
			80	-	736		
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	tRC= 125µs, /CAS = CBR cycling or 0.2V, /WE = VCC – 0.2V A0 - A10 = VCC – 0.2V or 0.2V DQ0 - DQ31 = VCC – 0.2V, 0.2V or open	Tras ≤ 300ns	-	6.4	mA	1,4,5
			tRAS ≤ 1¥ s	-	4.8		
ICC8	VCC Supply Current Self Refresh (SL-part only)	/RAS & /CAS ≤ 0.2V /OE & /WE & A0-A10= VCC-0.2V or 0.2V DQ0-DQ31= VCC-0.2V, 0.2V or open		-	2.7	mA	5
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5Ma		2.4	-	V	

NOTE
1. ICC1, ICC3, ICC4,ICC6 and ICC7 depend on cycle rate.
2. output loading. Specified values are obtained with the ouptup open.
3. ICC is specified as average current. For ICC1,ICC3 and ICC6 address can be changed maximum two times while /RAS=VIL. For ICC4, address can be changed maximum once while /CAS=VIH.
4. Only tRAS(max.)=1µs is applied to refresh of battery backup but tRAS(max.)=10µs is applied to normal functional operation.
5. ICC5(max.)=6.4mA, ICC7 and ICC8 are applied to SL-part only (HYM5332814ASLM/ASLTM/ASLMG/ASLTMG)

AC CHARACTERISTICS

(TA=0¡ ßto 70¡ ÉVCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1,2,3

#	SYMBOL	PARAMTER	HYM532814A M-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRPC	/RAS to /CAS Precharge Time	0	-	0	-	0	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tRHCP	Time from /CAS Precharge	35	-	40	-	45	-	ns	
5	tRAC	Access Time from /RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from /CAS	-	15	-	18	-	20	ns	4,9
7	tAA	Access Time from Coulmn Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from /CAS Precharge	-	35	-	40	-	45	ns	4
9	tCLZ	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	tRP	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	/RAS Pulse Width (EDO Mode)	60	125K	70	125K	80	125K	ns	
15	tRSH	/RAS Hold Time	15	-	18	-	20	-	ns	
16	tCSH	/CAS Hold Time	40	-	50	-	60	-	ns	
17	tCAS	/RAS Pulse Width	12	10K	15	10K	20	10K	ns	
18	tRCD	/RAS to /CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	/RAS to Column Address Delay Time	15	30	15	30	17	40	ns	10
20	tCRP	/CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	/CAS Precharge Time	8	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	12	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	10	-	15	-	ns	
26	tAR	Column Address Hold Time from /RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	10	-	15	-	ns	
32	tWCR	Write Command Hold Time from /RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to /RAS Lead Time	15	-	18	-	20	-	ns	
35	tCWL	Write Command to /CAS Lead Time	15	-	18	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	13	-	13	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to /RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		SL-part	-	256	-	256	-	256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMTER	HYM532814A M-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	t_{CSR}	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	t_{CHR}	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
43	t_{CPT}	/CAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
44	t_{WRP}	/WE to /RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	t_{WRH}	/WE to /RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	t_{RASS}	/RAS Pulse (Self Refresh)	100	-	100	-	100	-	ns	
47	t_{RPS}	/RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
48	t_{CHS}	/CAS Hold Time from /RAS (Self Refresh)	-50	-	-50	-	-50	-	ns	
49	t_{DOH}	Output Data Hold Time	3	-	3	-	3	-	ns	
50	t_{REZ}	Output Buffer Turn-off Delay (/RAS)	-	15	-	15	-	15	ns	5,15
51	t_{WPE}	Output Buffer Turn-off Delay (/WE)	-	15	-	15	-	15	ns	5
52	t_{WPE}	/WE Pulse Width for Output Disable	10	-	10	-	10	-	ns	
53	t_{WED}	/WE to Data Delay Time	15	-	15	-	15	-	ns	

NOTE :

1. An initial pause of 200§ Ás required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS intilization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If /RAS= Vss during power-up, the HYM532814A could begin an active cycle. This conditionn results in higher power-up current than necessary demands from the power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY5117404A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.(V_{OH}=2.0V, V_{OL}=0.8V)
5. t_{CEZ}(max.).t_{OEZ}(max.),t_{REZ}(max.) and t_{WEZ}(max.) define the time at which the output achiveds the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in late write or read-modify-write Cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throught the entire cycle
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Measured with the specified current load and 100pF.
12. A burst of 2048 /CAS-before-/RAS refresh cycles must bwe executed within 32ms after existing self refresh (for SL-part).
13. If $t_{CWD} \geq t_{WCS}$(min.) $t_{RWD} \geq t_{RWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neighter of the above conditions are met, the condition of the data out (at access time and until /CAS goes back to V_{IH}) is indeterminated.
14. In /CAS before /RAS self refresh mode.

    In case of using distributed /CAS before /RAS refresh, refresh 1024 times during a 256ms after reset

    In case of using burst /CAS before /RAS refresh, refresh 1024 times during a 32ms after reset

    In case of using /RAS only refresh, refresh against all refresh address during a 32ms after rese
15. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going.

    If /CAS goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.

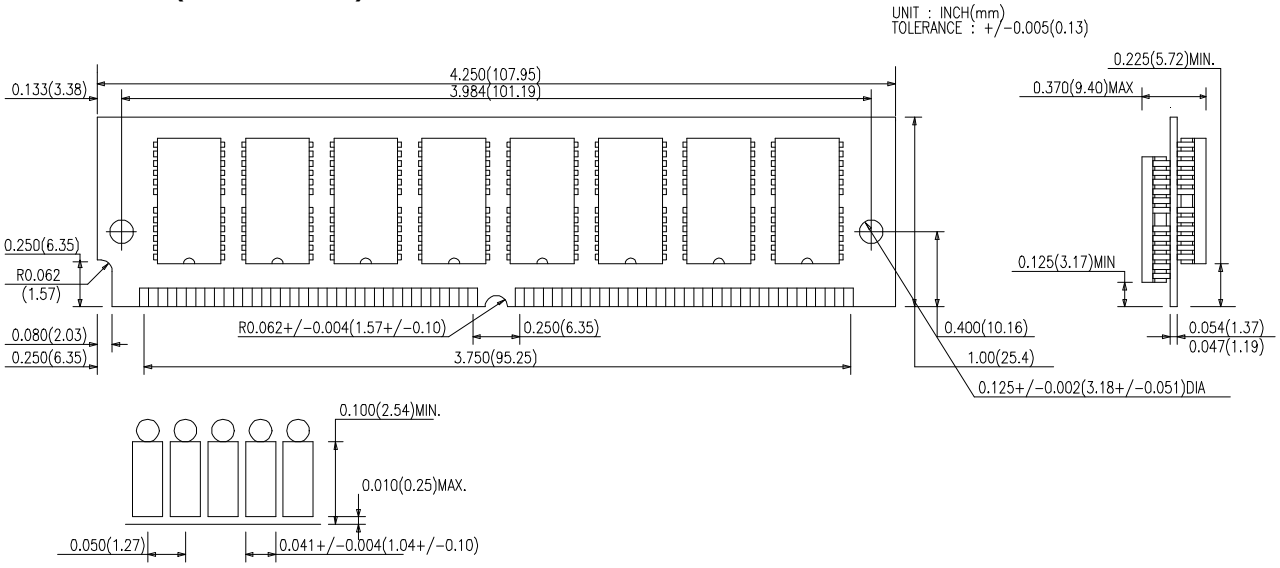
CAPACITANCE

(TA=25¡ ÉVcc=5V± 10%, Vss=0V, f=1MHz, unless otherwise noted.)

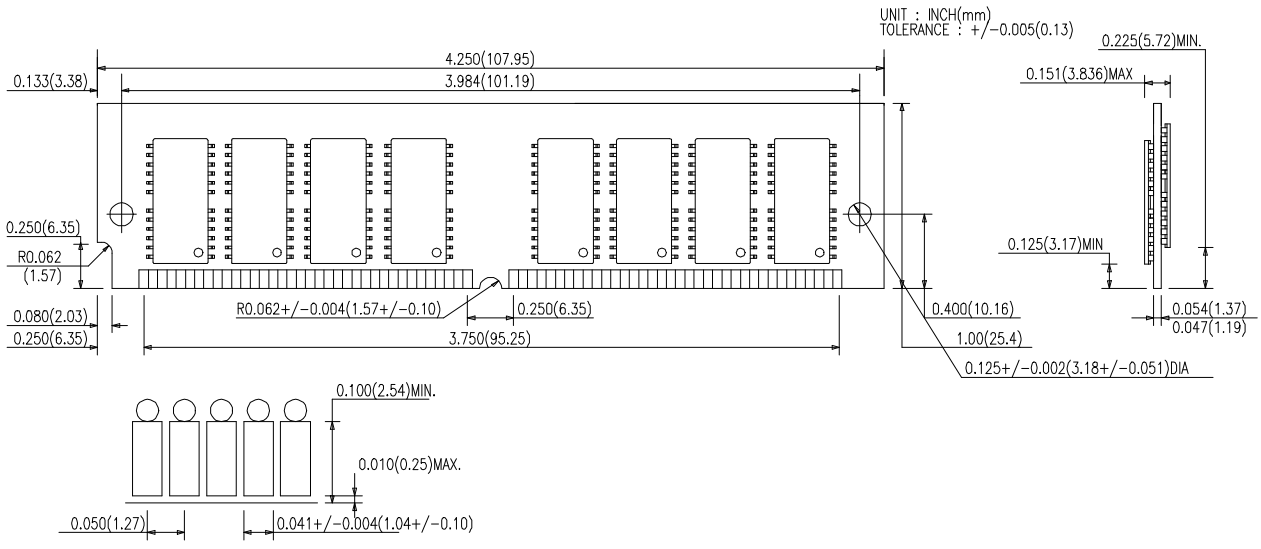
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	110	pF
C_{IN2}	Input Capacitance (/WE)	-	120	pF
C_{IN3}	Input Capacitance (/RAS0-/RAS3)	-	35	pF
C_{IN4}	Input Capacitance (/CAS0-/CAS3)	-	35	pF
C_{DQ}	Data Input/output Capacitance (DQ0-DQ31)	-	25	pF

PACKAGE DIMENSION

72pin Single Inline Memory Module (M; Tin-Lead plated, MG; Gold plated)
HYM532814A (SOJ Mounted)



HYM532814A (TSOPII Mounted)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532814AM	60/70/80		SIMM	Tin-Lead
HYM532814ASLM	60/70/80	SL-part	SIMM	Tin-Lead
HYM532814ATM	60/70/80		SIMM	Tin-Lead
HYM532814ASLTM	60/70/80	SL-part	SIMM	Tin-Lead
HYM532814AMG	60/70/80		SIMM	Gold
HYM532814ASLMG	60/70/80	SL-part	SIMM	Gold
HYM532814ATMG	60/70/80		SIMM	Gold
HYM532814ASLTMG	60/70/80	SL-part	SIMM	Gold