

- Fully Integrated Sonet/SDH Transceiver to Support Clock/Data Recovery and MUX/DEMUX Functions
- Supports OC-48, OC-24, OC-12, Gigabit Ethernet and OC-3 Data Rates With Auto Rate Detection
- Supports Transmit Only, Receiver Only, Full Transceiver and Repeater Functions in a Single Chip Through Configuration Pins
- Supports SONET/SDH Frame Detection
- On Chip PRBS Generation and Verification
- Supports 4-Bit LVDS (OIF99.102) Electrical Interface
- Parity Checking and Generation for the LVDS Interface
- Single 2.5 V Power Supply
- Interfaces to Backplane, Copper Cables or Optical Modules
- Hot Plug Protection
- Low Jitter PECL Compatible Differential Serial Interface With Programmable Preemphasis for the Serial Output
- On-Chip Termination for LVDS and PECL Compatible Interfaces
- Receiver Differential Input Thresholds 150 mV Minimum
- Supports SONET Loop Timing
- Low Power < 700 mW at OC-48 Rate
- ESD Protection >2 kV
- 155 MHz or 622 MHz reference Clock
- Maintains Clock Output in Absence of Data
- Local and Remote Loopback
- 100 Pin VQFP Package With PowerPAD™ Design

description

The SLK2501 is a single chip multirate transceiver IC used to derive high speed timing signals for SONET/SDH based equipment. The chip performs clock and data recovery, serial-to-parallel, parallel-to serial conversion and frame detection function conforming to the SONET/SDH standards.

Through the rate selection pins or the auto rate detection function, the device can be configured to operate under OC-48, OC-24, OC-12, or OC-3 data rates. A user selectable external reference clock operating at 622.08 MHz or 155.52 MHz is required for the recovery loop and it also provide a stable clock source in the absence of serial data transitions.

The SLK2501 accepts 4-bit LVDS parallel data/clock and generates a NRZ SONET/SDH compliant signal at OC-3, OC-12, OC-24, or OC-48 rates. It also recovers the data and clock from the serial SONET stream and demultiplexes it into 4-bit LVDS parallel data for full duplex operation. The serial interface is a low jitter, PECL compatible differential interface.

The SLK2501 provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback and PRBS (2⁷-1) generation and verification.

The device comes in a 100 pin VQFP package and requires a single 2.5 V supply with 3.3 V tolerant inputs on the control pins. The SLK2501 is very power efficient dissipating less than 700 mW at 2.488 Gbps, the OC-48 data rate and it is characterized for operation from –40°C to 85°C.



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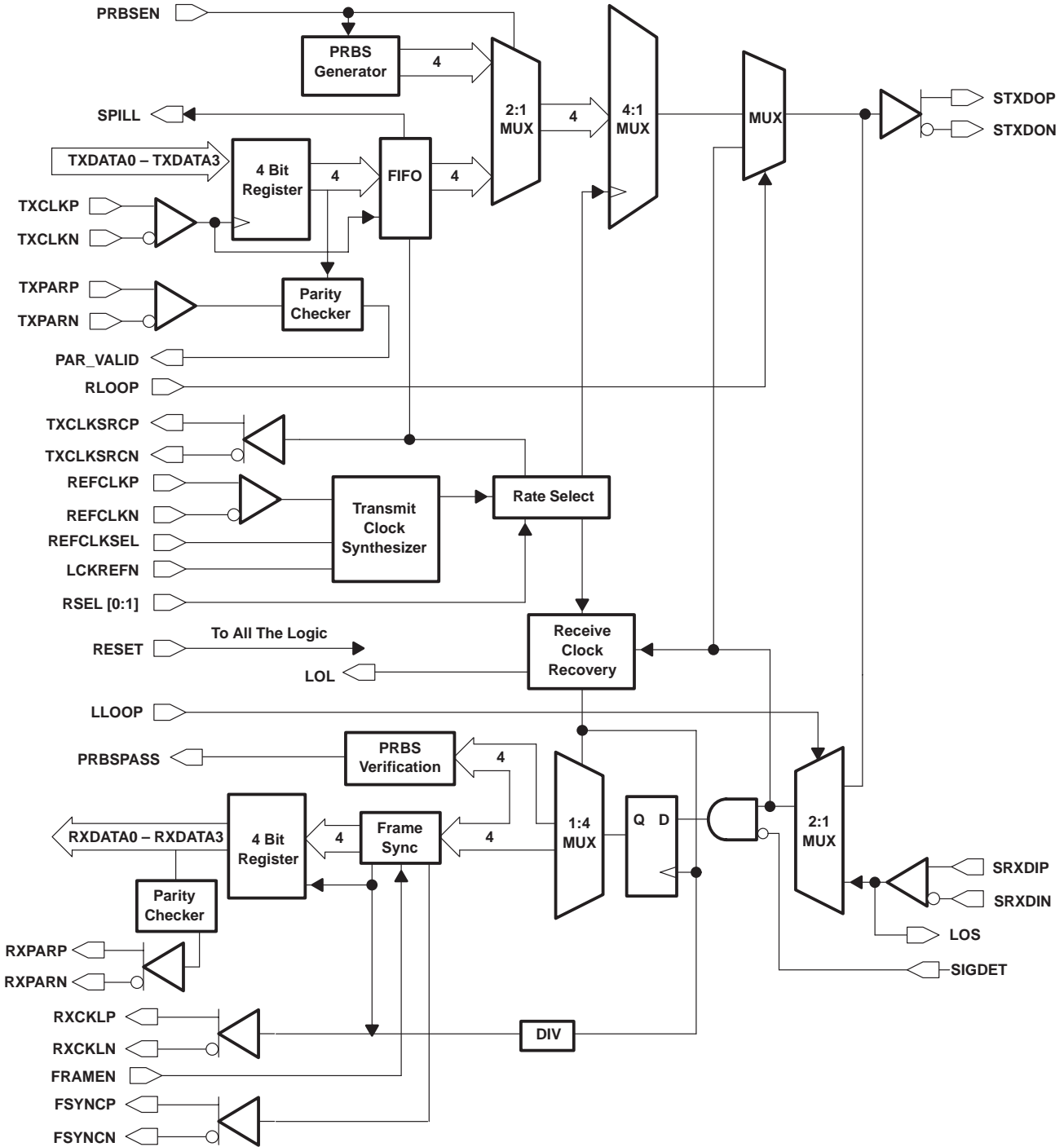
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SLK2501 OC-48/24/12/3 SONET/SDH MULTIRATE TRANSCEIVER

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block diagram



PRODUCT PREVIEW



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