Features

- 256KB, 512K and 1MB secondary cache module family for PowerPC^{TM}PReP/CHRP platforms
- Organized as a 32K, 64K or 128K x 72 package on a 5.06” x 1.10”, 182-lead, Dual Read-out DIMM
- Available in both linear (PowerPC^{TM}) burst mode and asynchronous SRAMs
- Fast access times: 9, and 11 with S-SRAM or 12ns with A-SRAM
- TAG access time: 10ns
- Low capacitive address, control, clock, and data bus loading
- Dual +3.3V and +5V, +/- 5% power supplies
- 5V-tolerant common data I/O
- Uses Burndy connector P/N ELF178KSC-3Z50 for Synchronous modules.
- Uses Burndy connector P/N ELF182JSC-3Z50 for Asynchronous modules.

Description

The IBM family of 256KB,512KB, and 1MB synchronous SRAM modules use IBM’s burstable, high performance 0.5 micron, CMOS Static RAMs . The 512KB and 1MB modules integrate four and eight 64K x 18 burst SRAMs respectively..The burst mode operation of these modules support PowerPC-based systems. Asynchronous modules of 256KB, 512KB and 1MB are also available. The asynchronous 256KB/512KB module uses 32Kx 8 ASRAMs, while the 1MB uses 128K x 8 ASRAMs .

The module also contains a 16K x 15 cache Tag RAM (IDT71216-10), allowing fast comparison of the twelve stored common I/O Tag bits and current Tag input data. An active Tag MATCH output is generated when these two groups of data are equal for a given address.

All A-SRAM modules are fully static designs eliminating the need for external clocks or strobes. However, the Tag RAM requires a clock (CLK2) for its operation. The output enable ($\overline{\text{SRAM\_OE}}$) feature provides increased system flexibility and eliminate Bus contention problems.

The Synchronous SRAM module is operated with dual +3.3V and +5V power supplies, whereas, the Asynchronous SRAM module operates with +5V power supply. The inputs and outputs are 5V tolerant and LVTTL compatible in both cases .

Connector Pin Assignment

GND	1	92	GND
PD0	2	93	PD1
PD2	3	94	PD3
DH30	4	95	DH31
DH28	5	96	DH29
DH26	6	97	DH27
DH24	7	98	DH25
VCC3.3	8	99	VCC3.3
DP3	9	100	SRAM_WE3
DH22	10	101	DH23
DH20	11	102	DH21
DH19	12	103	DH18
GND	13	104	GND
DH17	14	105	DH16
DP2	15	106	SRAM_WE2
DH15	16	107	DH14
DH12	17	108	DH13
VCC5	18	109	VCC5
DH11	19	110	DH10
DH9	20	111	DH8
DP1	21	112	SRAM_WE1
DH7	22	113	DH6
VCC3.3	23	114	VCC3.3
DH5	24	115	DH4
DH3	25	116	GND
DH2	26	117*	CLK0
DH0	27	118	GND
DP	28	119	DH1
GND	29	120	SRAM_WE0
CLK1	30*	121	DL31
GND	31	122	DL30
DL28	32	123	GND
DL26	33	124	DL29
DL24	34	125	DL27
DP7	35	126	DL25
VCC5	36	127	VCC5
DL22	37	128	SRAM_WE7
DL20	38	129	DL23
DL18	39	130	DL21
DL16	40	131	DL19
GND	41	132	GND
DP6	42	133	DL17
DL14	43	134	SRAM_WE6
DL12	44	135	DL15
DL11	45	136	DL13
GND	46	137	GND
DL9	47	138	DL10
DP5	48	139	DL8
DL7	49	140	SRAM_WE5
DL4	50	141	DL6
VCC3.3	51	142	VCC3.3
DL3	52	143	DL5
DL1	53	144	DL2
DL0	54	145	GND
GND	55	146*	CLK3
CLK2, (TAG)	56	147	GND
GND	57	148*	CLK4
DP4	58	149	GND
SRAM_OE0	59	150	SRAM_WE4
SRAM_OE1	60	151	SRAM_ALE
VCC3.3	61	152	VCC3.3
ADDR0_A	62	153	ADDR1_A
ADDR0_B	63	154	ADDR1_B
SRAM_ADS0	64*	155*	SRAM_CNT_EN0
SRAM_ADS1	65*	156*	SRAM_CNT_EN1
VCC5	66**	157**	VCC5
VCC5	67**	158**	VCC5
A28	68	159	A27
A26	69	160	A24
A25	70	161	A22
A23	71	162	A20
GND	72	163	GND
A21	73	164	A18
A19	74	165	A16
A17	75	166	A15
A13	76	167	A14
VCC3.3	77	168	VCC3.3
A12	78	169	A10
A11	79	170	A8
A9	80	171	A6
GND	81	172	GND
A7	82	173	A4
A5	83	174	A2
A3	84	175	A1
A0	85	176	RESERVED
VCC5	86	177	VCC5
TAG_CLR	87	178	TAG_VALID
TAG_MATCH	88	179	TAG_WE
TAG_OE	89	180	STANDBY
DIRTYIN	90	181	DIRTYOUT
GND	91	182	GND

NOTES:

* These pins are no connects for the asynchronous module version

** Synchronous modules do not have pins 66, 67, 157 and 158 (physical cut-out)

Pin Definition and Description

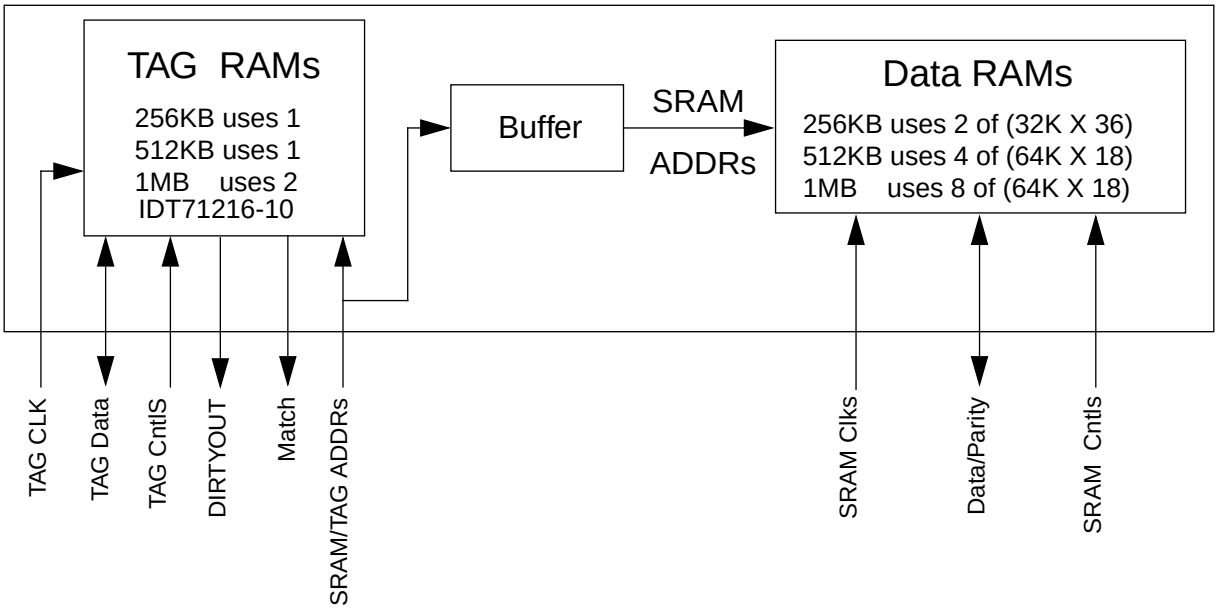
Signal	I/O	Number of Pins	Description
A0-A28	I	29	Address inputs (MSB:0, LSB:28)
ADDR0	I	2	Least significant address bit when asynchronous SRAMs are used
ADDR1	I	2	Next to least significant address bit when asynchronous SRAMs are used
DH0-DH31	I/O	32	High data bus (MSB:0, LSB:31)
DL0-DL31	I/O	32	Low data bus (MSB:0, LSB:31)
DP0-DP7	I/O	8	Data parity bus (MSB:0, LSB:7)
PD0/IDS_CLK	I	1	Presence detect bits 0 / EEPROM serial clock
PD1/IDS_DATA	I/O	1	Presence detect bits 1 / EEPROM serial data
PD2-PD3	O	2	Presence detect bits 2 and 3
$\overline{\text{SRAM\_ADS(0-1)}}$	I	2	SRAM address status control (ADSC) strobes
SRAM_ALE	I	1	SRAM address latch enable
$\overline{\text{SRAM\_CNT\_EN(0-1)}}$	I	2	SRAM burst advance control (ADV) enables
$\overline{\text{SRAM\_OE(0-1)}}$	I	2	SRAM output enables
$\overline{\text{SRAM\_WE(0-7)}}$	I	8	SRAM write enables (MSB:0, LSB:7)
$\overline{\text{TAG\_CLR}}$	I	1	Tag RAM clear
TAG_MATCH	O	1	Tag RAM match indication
TAG_VALID	I	1	Tag RAM valid bit
$\overline{\text{TAG\_WE}}$	I	1	Tag RAM write enable
$\overline{\text{TAG\_OE}}$	I	1	Tag RAM output enable
DIRTYIN	I	1	Dirty input bit
DIRTYOUT	O	1	Dirty output bit
STANDBY	I	1	Standby pin
RESERVED		1	Reserved pins
CLK0-CLK4	I	5	Clock inputs: CLK(0,1,3,4) are for SRAMs, CLK2 is for TagRAM For 512KB or less use CLK(0-2) only For 1MB use all the clocks
GND	I	24	Ground.
VCC3.3	I	10	+3.3V power supply
VCC5	I	10	+5V power supply

Ordering Information

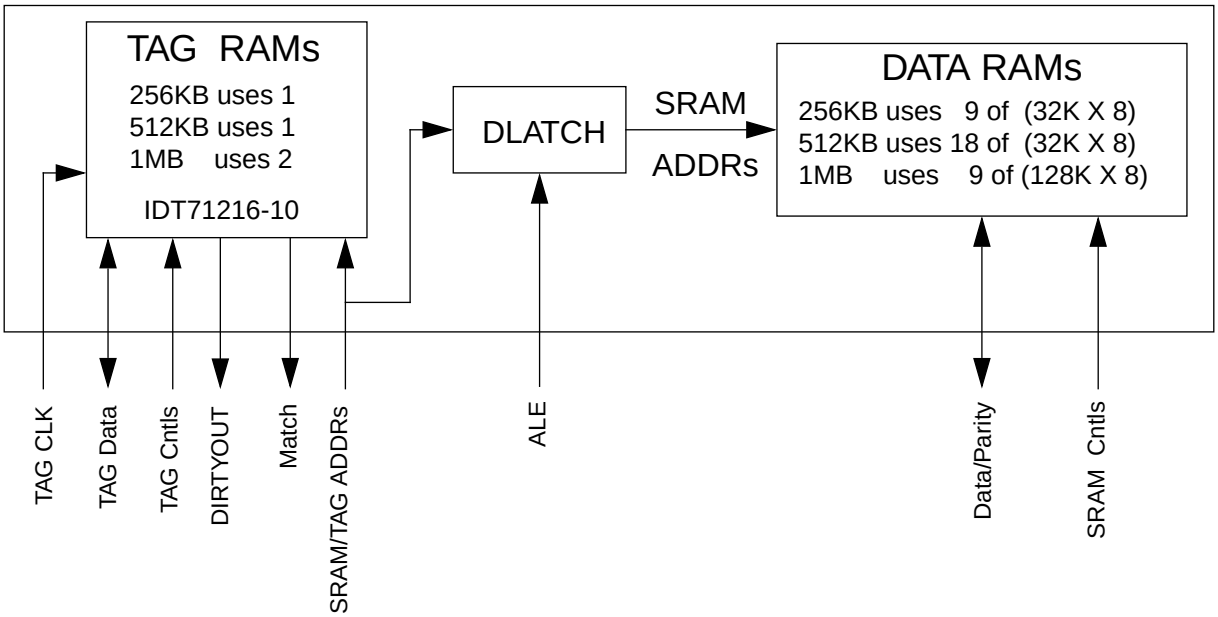
Part Number	Organization	Access / Cycle	Leads	Type	Availability
IBM14P64724DPA-9	64K x 72	9 ns / 15 ns	182	PowerPC	Now
IBM14P64724DPA-11	64K x 72	11 ns / 15 ns	182	PowerPC	Now
IBM14P13724DPA-9	128K x 72	9 ns / 15 ns	182	PowerPC	Now
IBM14P13724DPA-11	128K x 72	11 ns / 15 ns	182	PowerPC	Now
IBM14P32724FPA-9	32K x 72	9 ns / 15 ns	182	PowerPC	On Request
IBM14P32724FPA-11	32K x 72	11 ns / 15 ns	182	PowerPC	On Request
IBM14P32726BAA-12	32K x 72	12 ns / 15 ns	182	Async	Now
IBM14P64726BAA-12	64K x 72	12 ns / 15 ns	182	Async	Now
IBM14P13726BAA-12	128K x 72	12 ns / 15 ns	182	Async	Now

Block Diagram

Synchronous module (256KB, 512KB & 1MB):



Asynchronous module (256KB, 512KB & 1MB):



Burst Sequence Truth Table (linear burst) for IBM14P32724DPA,IBM14P64724DPA, IBM14P13724DPA

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(1,0)	(1,1)	(0,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(0,0)	(0,1)	(1,0)

Presence Detect Table

Part Number	Module Burst Type	Module Size	PD0	PD1	PD2	PD3
IBM14P32724FPA	Linear	256KB	GND	GND	Vcc3.3	GND
IBM14P64724DPA	Linear	512KB	Vcc3.3	GND	Vcc3.3	GND
IBM14P13724DPA	Linear	1MB	GND	Vcc3.3	Vcc3.3	GND
IBM14P32726BAA	Async	256KB	GND	GND	Vcc5	Vcc5
IBM14P64726BAA	Async	512KB	Vcc5	GND	Vcc5	Vcc5
IBM14P13726BAA	Async	1MB	GND	Vcc5	Vcc5	Vcc5

Absolute Maximum Ratings

P/N IBM14P32724FPA, IBM14P64724DPA, & IBM14P13724DPA				
Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage (3.3V)	$V_{cc3.3}$	-0.5 to 4.6	V	1
Power Supply Voltage (5V)	V_{cc5}	-0.5 to 7.0	V	1
Input Voltage		-0.5 to 6.0	V	1, 2
Output Voltage		-0.5 to V_{DD}+0.5	V	1, 2
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See “Pin Definition and Description” table on page 5 for Input/Output voltage symbols and definitions.

Recommended DC Operating Conditions (T_A=0 to 70°C)

P/N IBM14P32724FPA, IBM14P64724DPA, & IBM14P13724DPA						
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	$V_{cc3.3}$	3.135	3.3	3.465	V	1
Supply Voltage	V_{cc5}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3

1. All voltages referenced to GND. All $V_{cc3.3}$,V_{cc5} and GND pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)

Capacitance (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, f=1MHz) Maximum values

P/N IBM14P32724FPA, IBM14P64724DPA, & IBM14P13724DPA						
Parameter	Symbol	Test Condition	256KB	512KB	1MB	Units
Input Capacitance (Address)	C_{IN1}	V_{IN} = 0V	14	14	24	pF
Input Capacitance (Control, $\overline{OE}$)	C_{IN2}	V_{IN} = 0V	22	22	22	pF
Input Capacitance ($\overline{WE}$, $\overline{CE}$, CLK)	C_{IN3}	V_{IN} = 0V	12	12	12	pF
Data I/O Capacitance (DQ0-DQ71)	C_{OUT}	V_{OUT} = 0V	10	10	15	pF

Absolute Maximum Ratings

P/N IBM14P32726BAA, IBM14P64726BAA, & IBM14P13726BAA				
Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage (5V)	V_{cc5}	-0.5 to 7.0	V	1
Input Voltage		-0.5 to 6.0	V	1, 2
Output Voltage		-0.5 to V_{CC5}+0.5	V	1, 2
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See “Pin Definition and Description” table on page 5 for Input/Output voltage symbols and definitions.

Recommended DC Operating Conditions (T_A=0 to 70°C)

P/N IBM14P32726BAA, IBM14P64726BAA, & IBM14P13726BAA						
Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{cc5}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3

1. All voltages referenced to GND. All $V_{cc3.3}$,V_{cc5} and GND pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -2.0V (pulse width ≤ 4.0ns)

Capacitance (T_A=0 to +70°C, V_{DD}=3.3V ± 5%, f=1MHz) Maximum values

P/N IBM14P32726BAA, IBM14P64726BAA, & IBM14P13726BAA							
Parameter		Symbol	Test Condition	256KB	512KB	1MB	Units
Input Capacitance (Address)	A0-A1 A2-A1	C_{IN1}	V_{IN} = 0V	47 14	47 14	27 21	pF
Input Capacitance (Control, $\overline{OE}$)		C_{IN2}	V_{IN} = 0V	47	47	27	pF
Input Capacitance ($\overline{WE}$, CLK)		C_{IN3}	V_{IN} = 0V	8	8	8	pF
Data I/O Capacitance (DQ0-DQ71)		C_{OUT}	V_{OUT} = 0V	8	12	8	pF

DC Electrical Characteristics (T_A= 0 to +70°C,$V_{cc3.3}$= 3.3V ± 5%, V_{cc5} = 5V ± 5%)

IBM14P32724FPA, IBM14P64724DPA, & IBM14P13724DPA					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{cc15}		900/320 1050/370	mA	1
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	I_{SB}		100/50 200/100	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}		8	µA	
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}		8	µA	
Output High Level Output “H” Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output “L” Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current;1st set is for 14P32724 and 14P64724 $V_{cc3.3}$/V_{cc5} supplies ; 2nd set is 14P13724 $V_{cc3.3}$/V_{cc5} supplies

DC Electrical Characteristics (T_A= 0 to +70°C, V_{cc5} = 5V ± 5%)

IBM14P32726BAA, IBM14P64726BAA, & IBM14P13726BAA					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{cc12}		1680/1970	mA	1
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	I_{SB}		290/580	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}		15	µA	
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}		15	µA	
Output High Level Output “H” Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output “L” Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

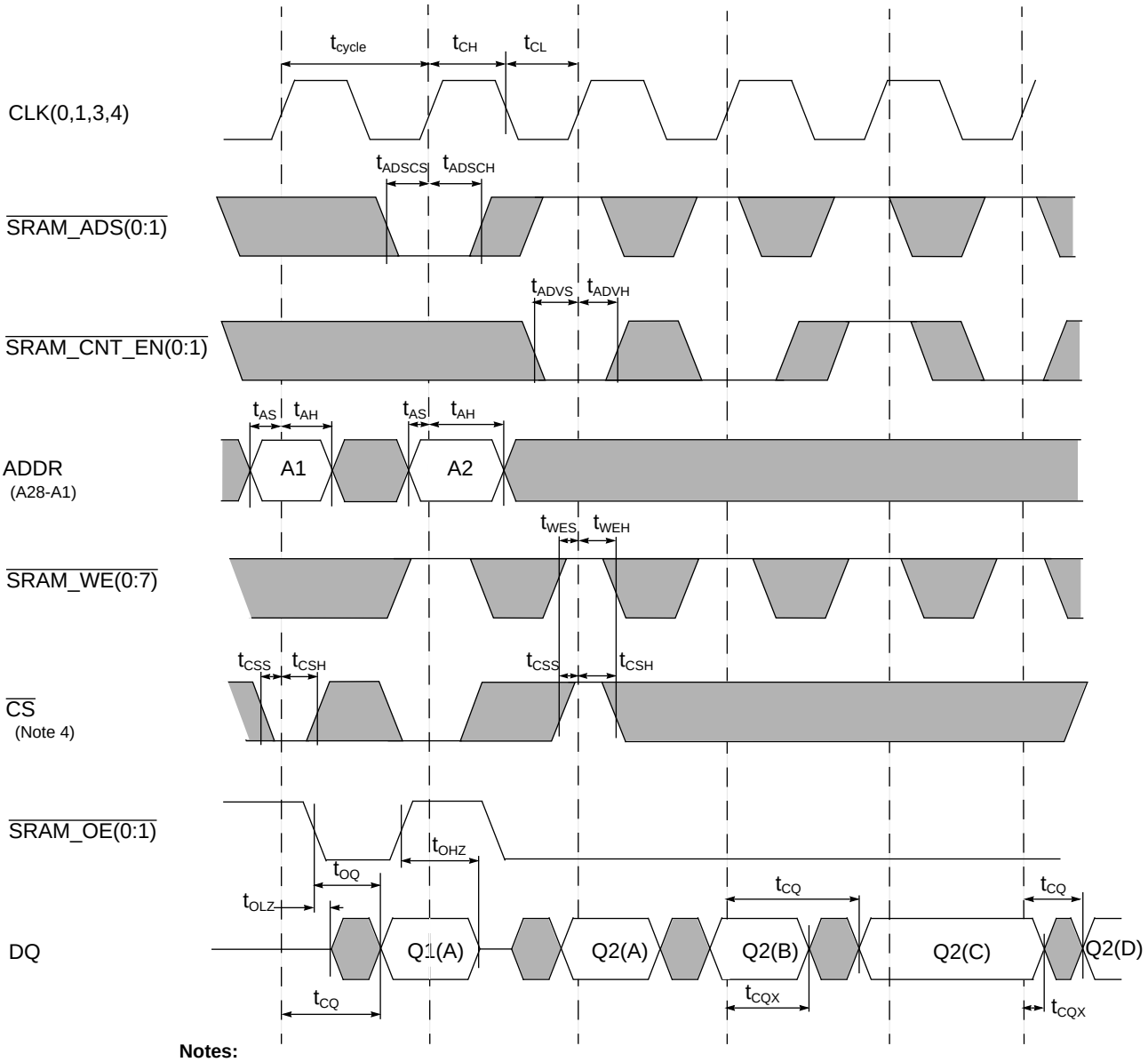
AC Characteristics (T_A=0 to +70°C, V_{CC3}=3.3V ± 5%, V_{CC5}=5.0V ± 5%Units in nsec)

P/N IBM14P32724FPA, IBM14P64724DPA and IBM14P13724DPA						
Parameter	Symbol	-9		-11		Notes
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	15.0	—	15.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	9.0	—	11.0	
Address Status Controller Setup Time	t_{ADSCS}	2.5	—	2.5	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.5	—	2.5	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.5	—	2.5	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.5	—	2.5	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.5	—	2.5	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.5	—	2.5	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	
Clock High to Output High Z	t_{CHZ}	—	5.0	—	5.5	1, 2
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	1, 2
Output Enable to High Z	t_{OHZ}	2.0	5.5	2.0	6.5	1
Output Enable to Low Z	t_{OLZ}	0.25	—	0.25	—	1
Output Enable to Output Valid	t_{OQ}	—	5.0	—	6.0	

1. Transitions are measured ± 200 mV from steady state voltage.
2. At any given voltage and temperature, T_{CHZ} max is always less than T_{CLZ} min for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from HIZ to new RAM data.

Synchronous SRAM Timing Diagram (Burst Read)

(IBM14P32724FPA, IBM14P64724DPA & IBM14P13724DPA)

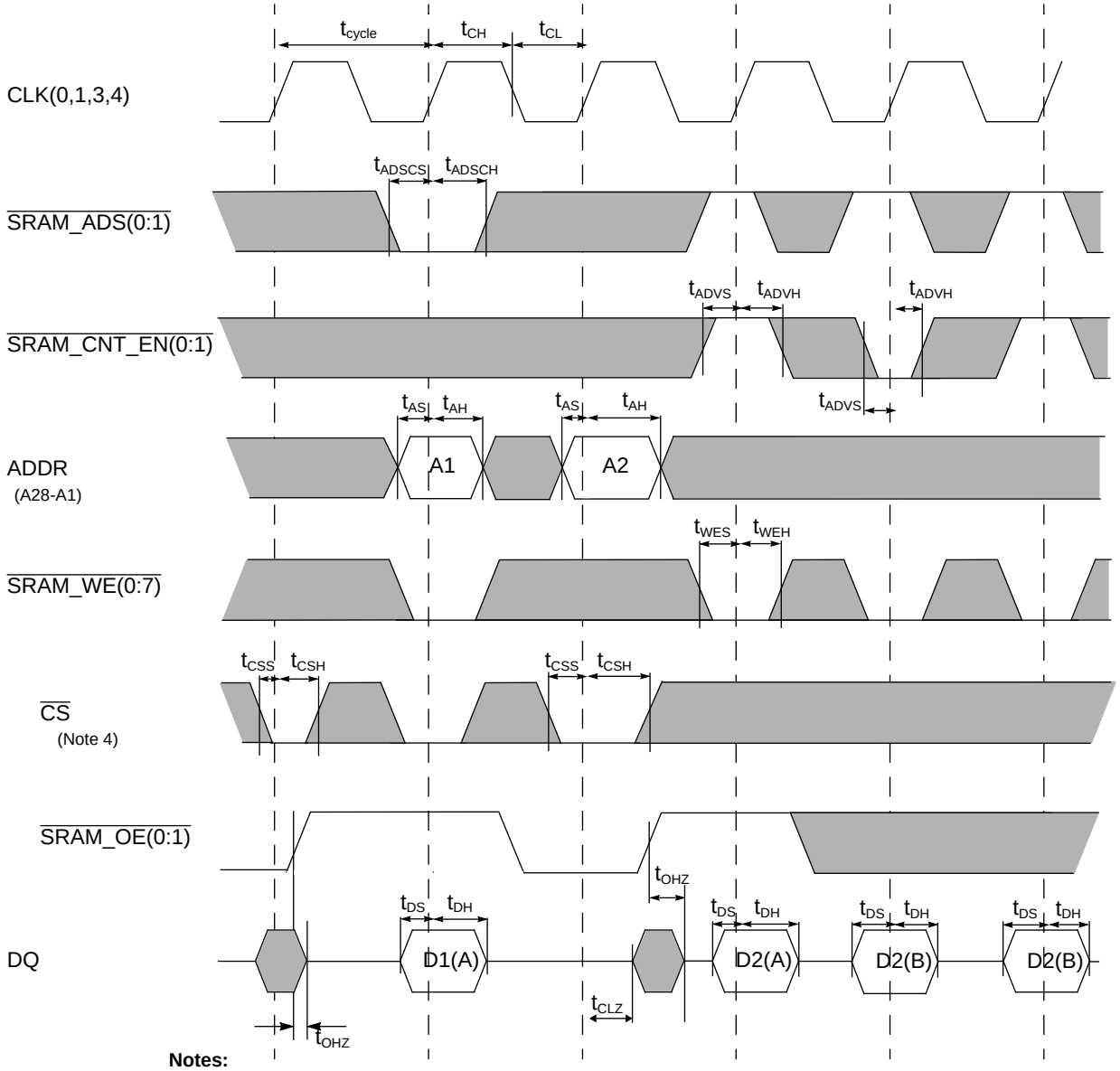


Notes:

1. Q1(A) and Q2(A) refer to output for Address A1 and A2 respectively.
2. Q2(B),Q2(C) and Q2(D) refer to output from subsequent internal burst counter addresses.
3. $\overline{\text{ADSP}}$ - Processor address status pin is tied high internal to the module.
4. $\overline{\text{CS}}$ - Address A12 serves as chip select for P/N 14P13724; standby pin serves as chip select for P/N 14P64724 and

Synchronous SRAM Timing Diagram (Burst Write)

(IBM14P64724DPA & IBM14P13724DPA)

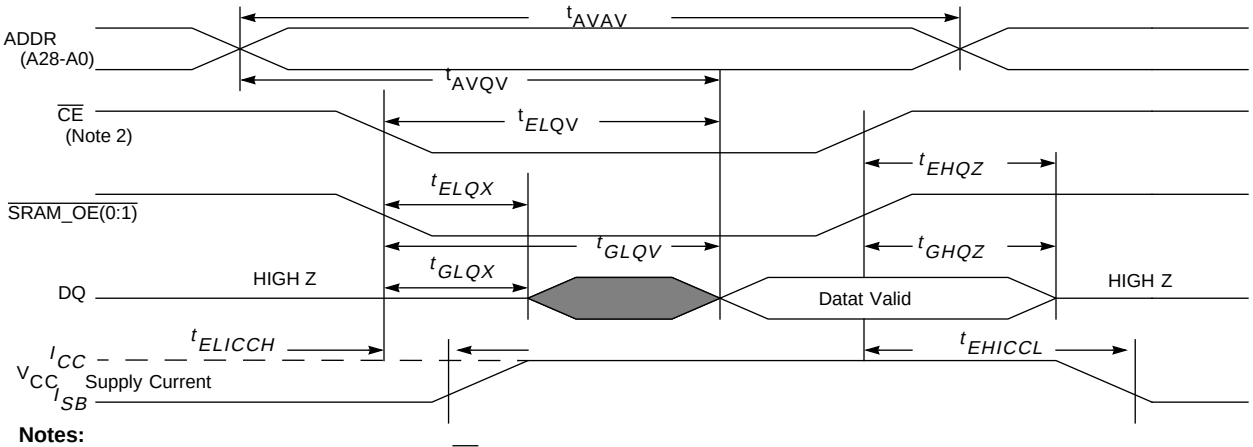


Notes:

1. D1(A) and D2(A) refer to data written to addresses A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3. $\overline{\text{ADSP}}$ - Processor address status pin is tied high internal to the module
4. $\overline{\text{CS}}$ - Address A12 serves as chip select for P/N 14P13724; standby pin serves as chip select for P/N 14P64724 and 14P32724.

Asynchronous SRAM Timing Diagram (Read)

(IBM14P32726BAA, IBM14P64726BAA and IBM14P13726BAA only)



Notes:

1. Addresses valid prior to or coincident with $\overline{CE}$ going low.
2. $\overline{CE}$ - Address A13 serves as $\overline{CE}$ for P/N 14P64726; STANDBY pin serves as CE for P/N 14P13726

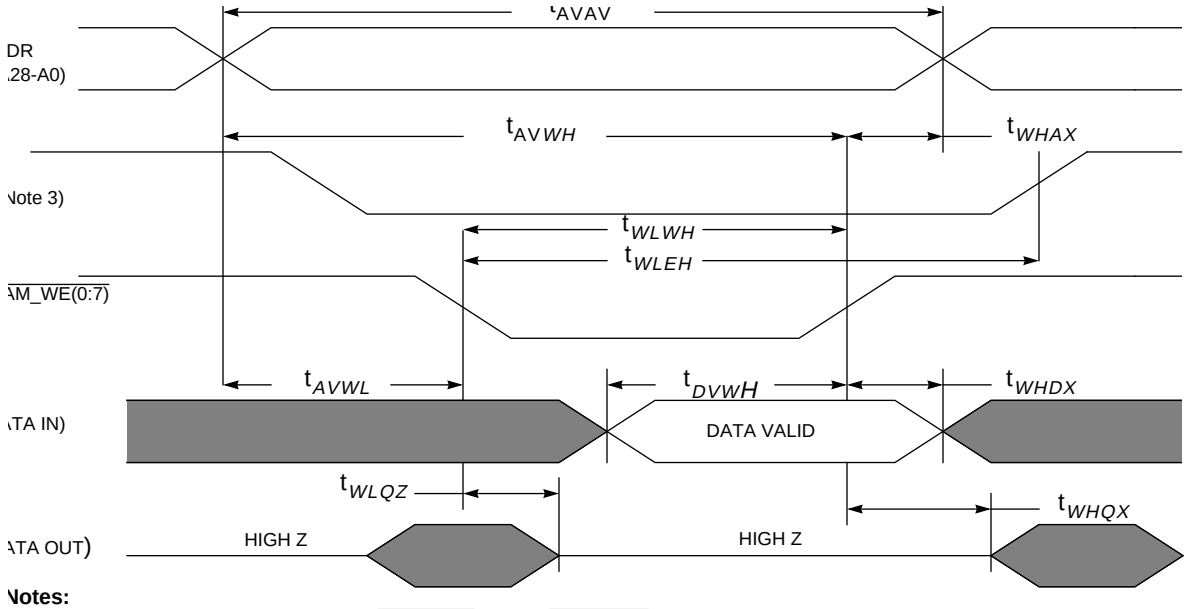
Read Cycle

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{AVAV}	12		ns	2
Address Cycle Time	t_{AVQV}		12	ns	
Enable Access Time	t_{ELQV}		12	ns	3
Output Enable Access Time	t_{GLQV}		6	ns	
Output Hold from Address Change	t_{AXQX}	3		ns	4, 5, 6
Enable Low to Output Active	t_{ELQX}	4		ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	0	7	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0		ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	0	6	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0		ns	
Power Down Time	t_{EHICCL}		12	ns	

1. $\overline{SRAM\_WE(0:7)}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{CE}$ going low
4. At any given voltage and temperature, t_{EHQZ} (max) is less than t_{ELQX} (min), and t_{GHQZ} (max) is less than t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured +/- 500 mv from steady-state voltage.
6. This parameter is sampled and not 100% tested..

Asynchronous SRAM Timing Diagram (Write Cycle 1)

(IBM14P32726BAA, IBM14P64726BAA and IBM14P13726BAA only)



Notes:

1. A write occurs during the overlap of $\overline{\text{SRAM\_OE}}$ low and $\overline{\text{SRAM\_WE}}$ low..
2. If $\overline{\text{SRAM\_OE}}$ goes low coincident with or after $\overline{\text{SRAM\_WE}}$ goes low, the output will remain in a high impedance state.
3. $\overline{\text{CE}}$ - Address A13 serves as $\overline{\text{CE}}$ for P/N 14P64726; STANDBY pin serves as CE for P/N 14P13726.

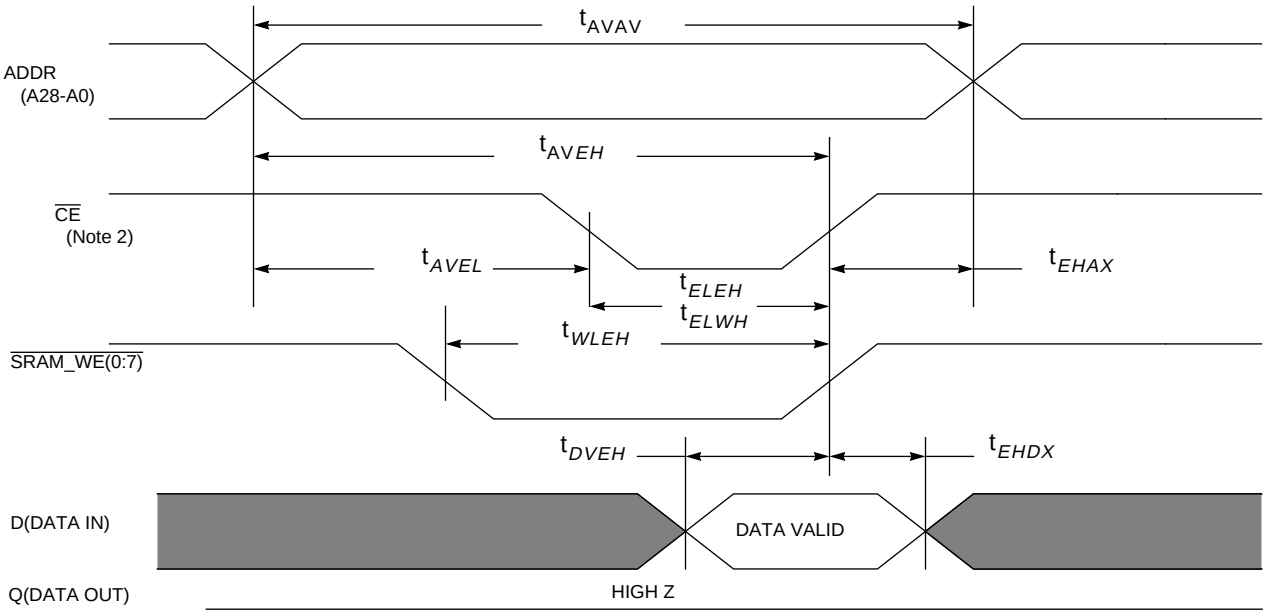
Write Cycle 1 ($\overline{\text{WE}}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	1
Address Setup Time	t_{AVWL}	0		ns	
Address Valid to End of Write	t_{AVWH}	10		ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	10		ns	
Write Pulse Width $\overline{\text{G}}$ High	t_{WLWH} t_{WLEH}	9		ns	2
Data Valid to End of Write	t_{DVWH}	6		ns	
Data Hold Time	t_{WHDX}	0		ns	
Write Low to Output High-Z	t_{WLQZ}	0	6	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	2		ns	3, 4, 5
Write Recovery Time	t_{WHAX}	0		ns	

1. All timings are referenced from the last valid address to the first transitioning address.
2. If $\overline{\text{SRAM\_OE}}$ is larger than or equal to V_{IH}, the output will remain in a high impedance state
3. At any given voltage and temperature , t_{WLQZ} (max) is less than t_{WHQX} (min), both for a given device and from device to device.
4. Transistion is measured ±500 mv from steady state voltage.
5. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 2)

(IBM14P32726BAA, IBM14P64726BAA and IBM14P13726BAA only)



Notes:
1. A write occurs during the overlap of $\overline{\text{SRAM\_OE}}$ low and $\overline{\text{SRAM\_WE}}$ low.
2. $\overline{\text{CE}}$ - Address A13 serves as $\overline{\text{CE}}$ for P/N 14P64726; STANDBY pin serves as CE for P/N 14P13726.

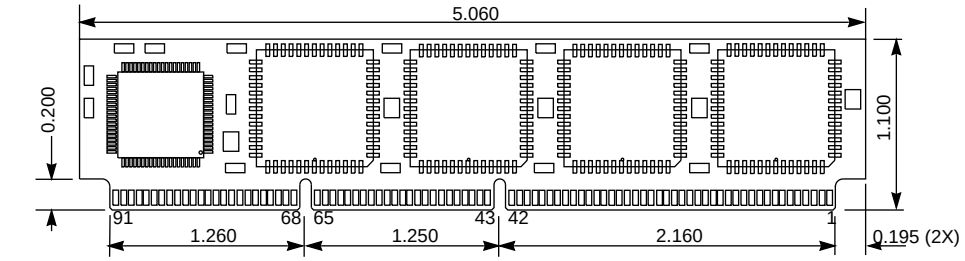
Write Cycle 2 ($\overline{\text{OE}}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	
Address Setup Time	t_{AVEL}	0		ns	
Address Valid to End of Write	t_{AVEH}	10		ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	9		ns	3, 4
Data Valid to End of Write	t_{DVEH}	6		ns	
Data Hold Time	t_{EHDX}	0		ns	
Write Recovery Time	t_{EHAX}	0		ns	

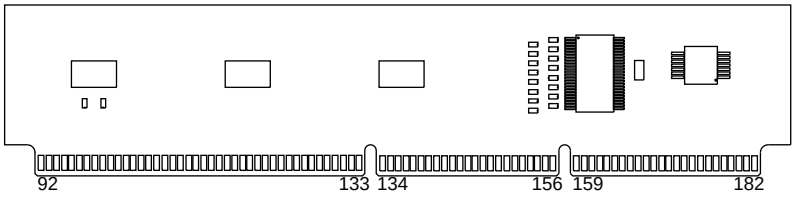
1. A write occurs during the overlap of $\overline{\text{SRAM\_OE}}$ low and $\overline{\text{SRAM\_WE}}$ low
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{\text{SRAM\_OE}}$ goes low coincident with or after $\overline{\text{SRAM\_WE}}$ goes low, the output will remain in a high impedance state.
4. If $\overline{\text{SRAM\_OE}}$ goes high coincident with or before $\overline{\text{SRAM\_WE}}$ goes high, the output will remain in a high impedance state.

Layout Drawing 512KB (/64K x 72), 182-pin Synchronous module

Front view:



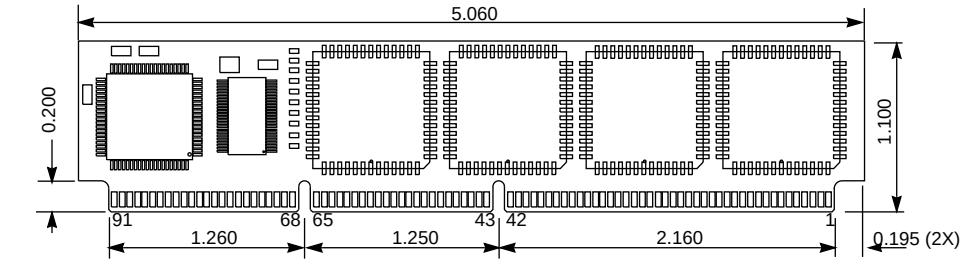
Back view:



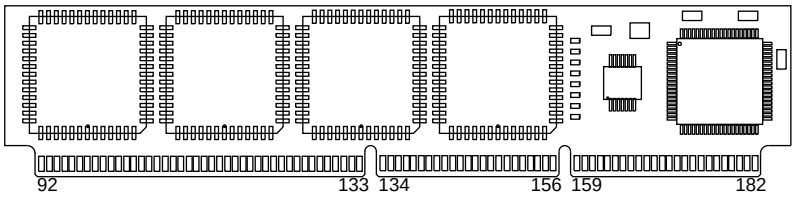
Uses Burndy connector: P/N ELF178KSC-3Z50

Layout Drawing 1MB (128K x 72), 182-pin Synchronous module

Front view:



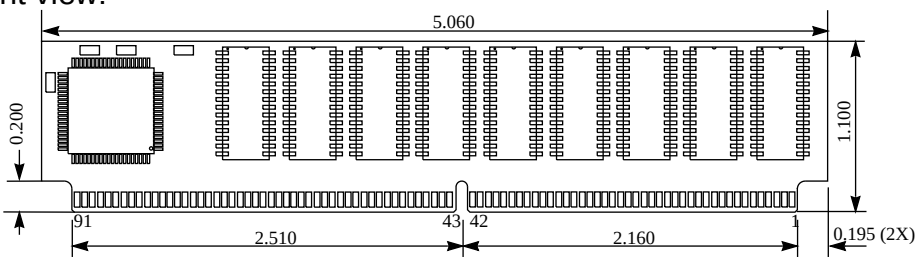
Back view:



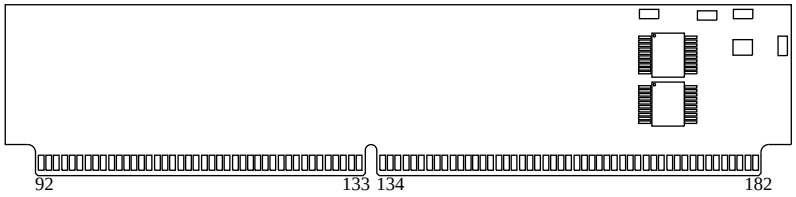
Uses Burndy connector: P/N ELF178KSC-3Z50

Layout Drawing 256KB (32K x 72), 182-pin Asynchronous module

Front view:



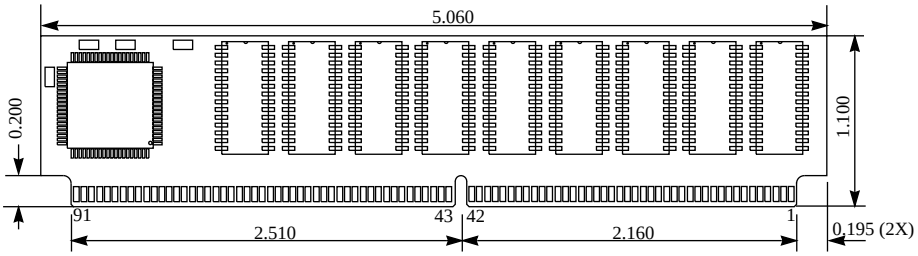
Back view:



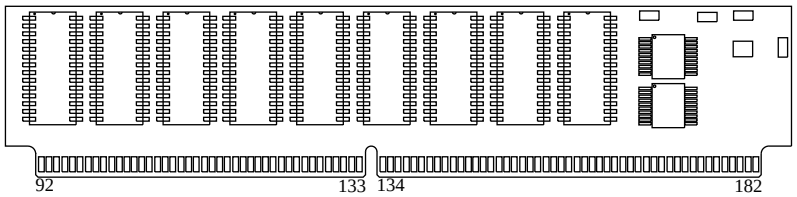
Uses Burndy connector: P/N ELF182JSC-3Z50

Layout Drawing 512KB (64K x 72), 182-pin Asynchronous module:

Front view:



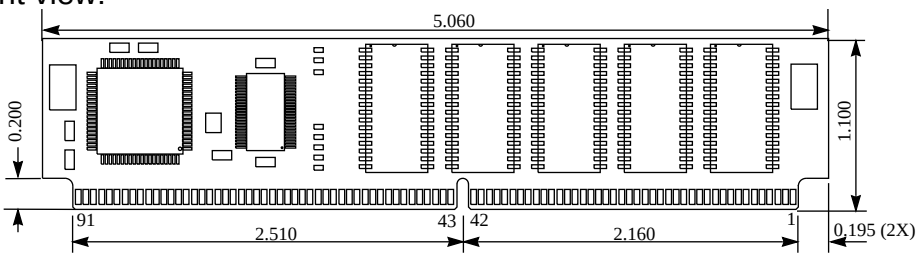
Back view:



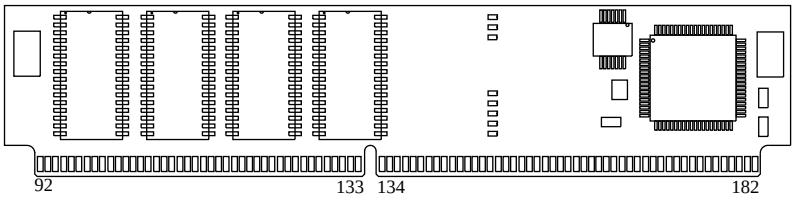
Uses Burndy connector: P/N ELF182JSC-3Z50

Layout Drawing 1MB (128K x 72), 182-pin Asynchronous module:

Front view:



Back view:



Uses Burndy connector: P/N ELF182JSC-3Z50

Revision Log

Rev	Contents of Modification
9/95	Preliminary Version
12/95	Latest Version; EC # E21059, Dt 12/05/95
3/96	Added 256KB SSRAM DIMMs P/Ns,Dt 03/07/96

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