SPICE Device Model Si6923DQ

P-Channel Rated MOSFET + Schottky Diode

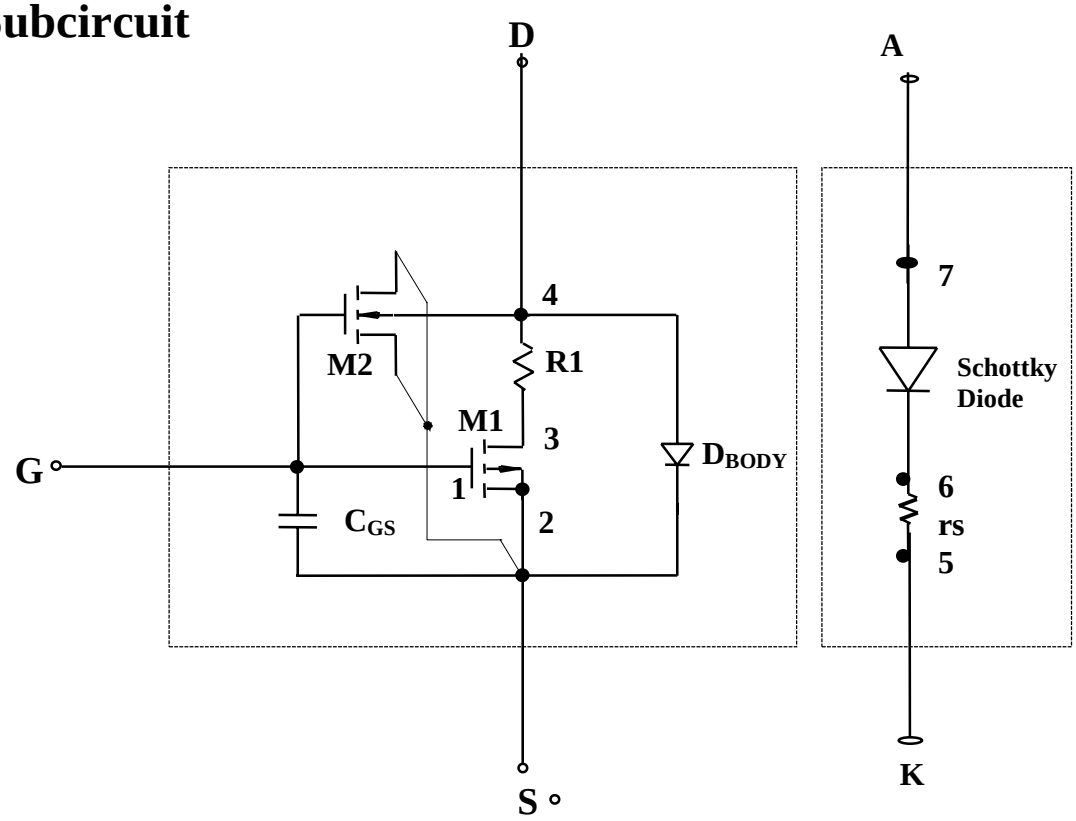
Characteristics

- P-Channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Modes
- Applicable Over a -55 to 125 ^{o} C Temperature Range
- Models Gate Charge, Transient and Diode Reverse Recovery Characteristics

Description

The attached SPICE model describes typical electrical characteristics of the Si6923DQ p-channel vertical trench-gated DMOS and the Schottky Diode. The subcircuit model was extracted and optimized over a 25 ^{o} C to 125 ^{o} C temperature range under pulse conditions for 0 to 5 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitance network is used to model gate charge characteristics while avoiding convergence problems of switched Cgd models. Model parameters values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

Model Subcircuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designer should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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P-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typ	Unit
Static				
Gate Threshold Voltage	V_{GS}(th)	V_{DS} = V_{GS}, I_D = -250µA	-.898	V
On-State Drain Current[a]	I_D(on)	V_{DS} = -5 V, V_{GS} = -4..5 V	74.3	A
Drain-Source On-State Resistance[a]	r_{DS}(on)	V_{GS} = -4.5 V, I_D = -3.5 A	0.0375	Ω
		V_{GS} = -2.5 V, I_D = -2.7 A	0.0572	
Forward Transconductance[a]	gfs	V_{DS} = -10 V, I_D = -3.5 A	11.5	S
Forward Voltage[a]	V_{SD}	I_F =I_S = -1.25 A, V_{GS} = 0V	0.815	V
Dynamic				
Input Capacitance	Ciss	V_{GS} = 0 V, V_{DS}=-10 V, f=1MHz	1950	pF
Output Capacitance	Coss		316	
Reverse Transfer Capacitance	Crss		128	
Total Gate Charge[b]	Qg	V_{DS} = -10 V, V_{GS}= -4.5 V I_D = -3.2 A	13.3	nC
Gate-Source Charge[b]	Qgs		2.8	
Gate-Drain Charge[b]	Qgd		2.9	
Turn-On Delay Time[b]	$t_{d(on)}$	V_{DD} = -10 V, R_L= 10 Ω I_D ≅ -1 A, V_{GEN} = -4.5 V, R_G = 6 Ω	14.8	ns
Rise Time[b]	t_r		13.8	
Turn-Off Delay Time[b]	$t_{d(off)}$		61.8	
Fall Time[b]	t_f		16.2	
Schottky Diode				
Forward Voltage Drop	Vf	IF= 1A	0.45	V
Junction Capacitance	CT	Vr=10 v	60	pf

Notes:
a. Pulse test: Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%
b. Independent of operating temperature.

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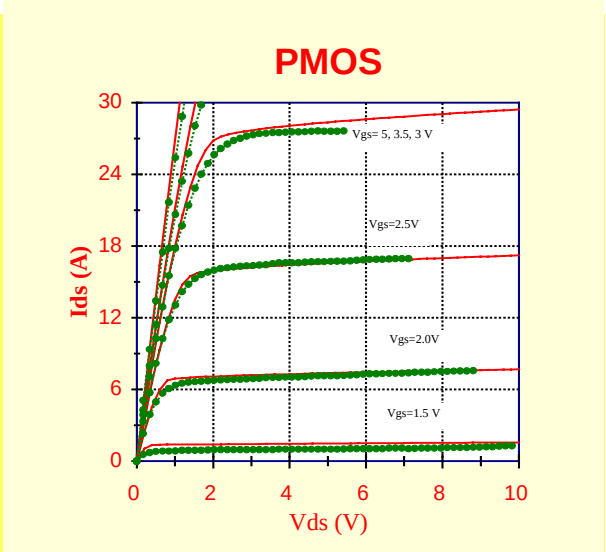
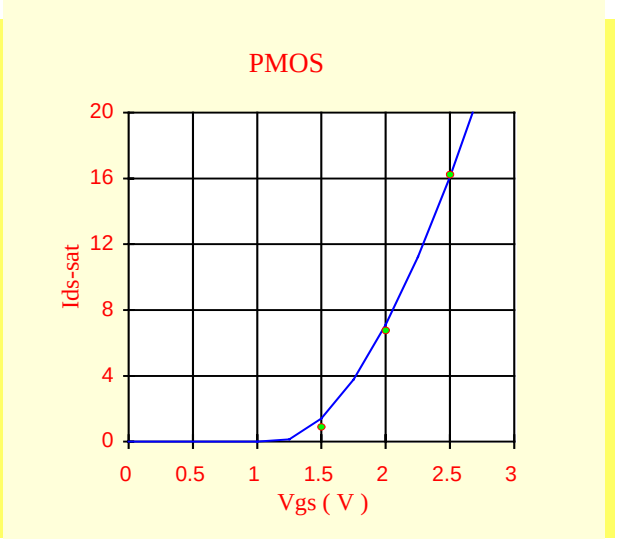
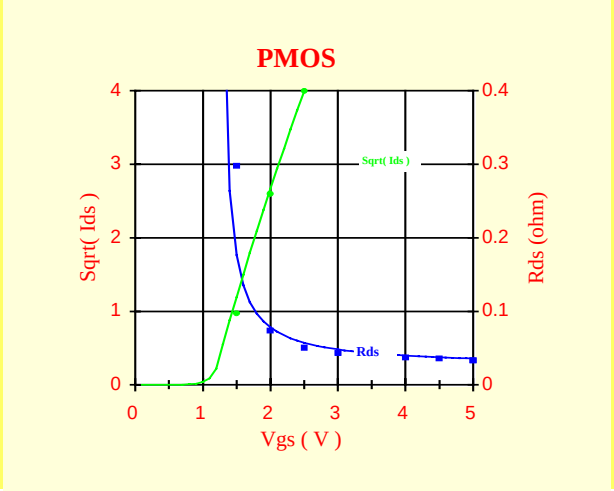
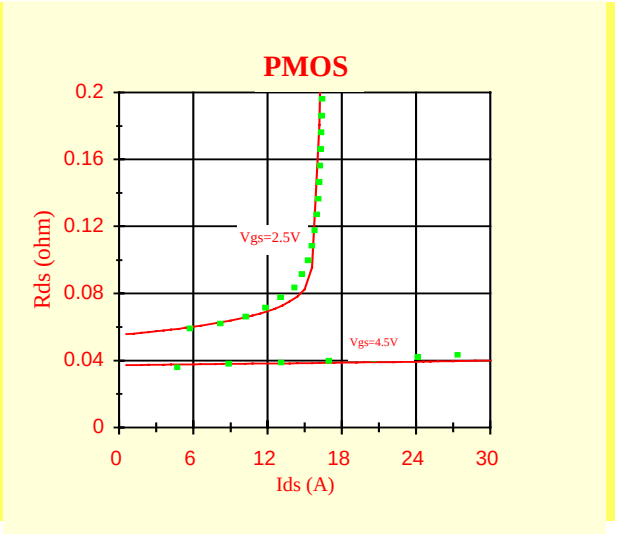
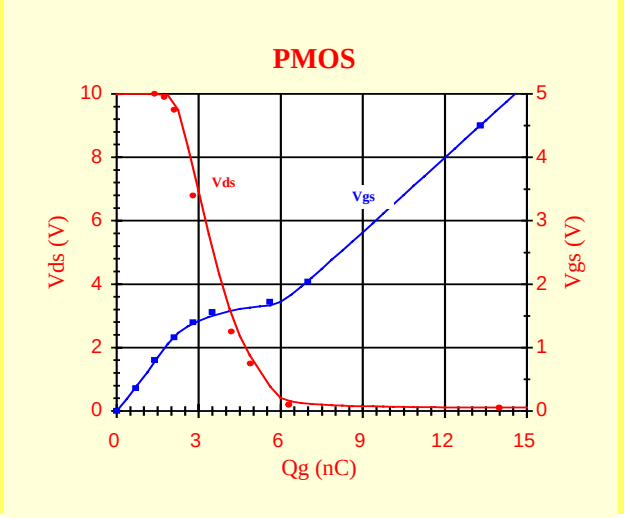
Comparison of Model with Measured Data

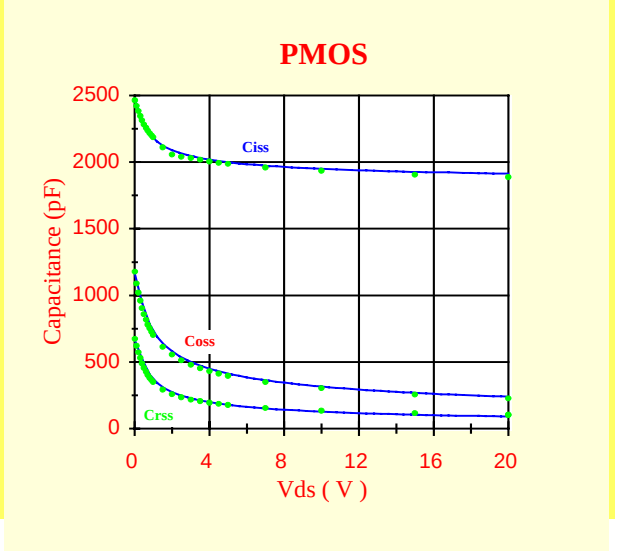












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Comparison of Model with Measured Data
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